Welcome to the electronic packaging’s premier conference!

ECTC 2013
The 63rd Electronic Components and Technology Conference
May 28-31, 2013
The Cosmopolitan of Las Vegas
Nevada, USA

Sponsored by:

Supported by:

For more information, visit: www.ectc.net
ELECTRONIC COMPONENTS AND TECHNOLOGY CONFERENCE
MAY 28 – 31, 2013
LAS VEGAS, NEVADA

Dear Friends,

As Mayor of the great City of Las Vegas, it is a pleasure to welcome you to the 2013 Electronic Components and Technology Conference at the Cosmopolitan.

Las Vegas continues to capture the world’s imagination as a city where anything is possible. With world-class hotels, award-winning restaurants, luxurious spas, fantastic shopping, the finest golf courses, and spectacular entertainment, Las Vegas remains one of the most electrifying destinations in the world.

While visiting or relocating to our City, it is my hope that you will have a chance to explore Downtown Las Vegas, an area of our City that is undergoing a dramatic renaissance. It is evolving into a vibrant place for living, working, entertainment, and the arts. Downtown Las Vegas is comprised of an enticing mix that includes:

- The neon-drenched excitement of the Fremont Street Experience, visited by over 21 million people each year.
- Multi-million dollar casinos and hotel renovations and expansions.
- Fremont East Entertainment District featuring trendy new gathering places for dining, dancing, cocktails and enjoyment.
- An emerging eclectic mix of live-in artists and galleries known as the 18b Arts District.
- Symphony Park, a phenomenal 61-acre planned development anchored by two key projects, the Cleveland Clinic Lou Ruvo Center for Brain Health, designed by renowned architect Frank Gehry, and The Smith Center for the Performing Arts, Las Vegas’ first world-class performing arts facility.
- A collection of world-class museums including the Neon Museum Boneyard, which holds over 100 donated and rescued Las Vegas signs that date from the late 1930s through the early 90s; the Mob Museum, which provides a fascinating glimpse into our City’s history; and the Discovery Children’s Museum in Symphony Park, among others.

Please take this opportunity to enjoy all that our grand City has to offer. Again, best wishes for a joyful, productive, and memorable conference.

Sincerely,

Carolyn G. Goodman
Mayor, City of Las Vegas

Welcome from the Mayor of Las Vegas
On behalf of the Program Committee and Executive Committee, it is my pleasure to welcome you to the 63rd Electronic Components and Technology Conference (ECTC) at The Cosmopolitan of Las Vegas, Nevada, USA. This premier international conference is sponsored by the IEEE Components, Packaging and Manufacturing Technology Society (CPMT).

The ECTC Program Committee represents a wide range of disciplines and expertise from the electronics industry around the world. We have selected more than 300 high-quality papers to be presented at the conference in 36 oral sessions, four interactive presentation sessions, and one student posters session. The 36 oral sessions cover papers on 3D/TSV, embedded devices, LEDs, Co-Design, RF packaging, and electrical and mechanical modeling, in addition to topics such as advanced packaging technologies, all types and levels of interconnections, materials, assembly manufacturing, system packaging, optoelectronics, reliability, MEMS, and sensors. The program committee strives to address new trends as well as ongoing technological challenges. Four Interactive Presentation sessions feature technical presentations in a format that enhances and encourages interaction. One student poster session focuses on research conducted in academia presented by the emerging scientists. Authors from companies, research institutes, and universities from over 25 countries will present at the ECTC, making it a truly diverse and global conference.

In addition to the technical sessions, panel and special sessions focusing on crucial topics presented by industry experts enhance the technical program. In the special session titled “The Role of Wafer Foundries in Next Generation Packaging,” held Tuesday, May 28, at 10 a.m., session chair Sam Karikalan will gather a panel of experts to present and discuss their proposed business models and strategies for embracing the next generation packaging needs of the industry. Key questions on cost, technology, assembly expertise and industry growth will be raised for the wafer foundries to address. Another special session will be held on Tuesday and will address “Modeling and Simulation Challenges in 3D Systems.” This session co-chaired by Yong Liu and Dan Oh is made up of keynote speakers as well as highlighted 3D modeling papers and will be held at 2 p.m. The Panel Discussion on Tuesday evening at 7:30 p.m., chaired by Ricky Lee and Kouchi Zhang titled “LED for Solid-State Lighting – For a Brighter Future,” will discuss emerging LED packaging technologies and market trends. The Plenary Session on Wednesday at 7:00 p.m., chaired by Lou Nicholls and titled “Packaging Challenges Across the Wireless Market Supply Chain,” will unveil the latest challenges of this growing industry with speakers from across the supply chain. Thursday evening starts with the Gala Reception at 6:30 p.m. and is followed by the CPMT Seminar at 8:00 p.m., which is titled “Advanced Low Loss Dielectric Materials for High Frequency and High Bandwidth Applications” and chaired by Kishio Yokouchi and Venky Sundaram.

The Professional Development Courses (PDCs), organized by the PDC Committee chaired by Kitty Pearsall, will be taught on Tuesday, May 28 (8:00 a.m.-5:30 p.m.). World-class experts in their fields offer 16 courses on different topics. Participants can catch up on new technology developments and broaden their technical knowledge base. The technical program and professional development courses are supplemented by the Technology Corner Exhibits where leading companies, primarily in the electronics components, materials, and packaging fields exhibit their latest technologies and products. The exhibitors invite you to their reception on Wednesday at 5:30 p.m. Along with our receptions and coffee breaks every day, luncheons are another great opportunity to network and discuss technical and business matters. It is my pleasure to announce that Dr. Chris Welty of IBM will be the invited keynote speaker at the ECTC Luncheon on Wednesday.

ECTC offers many opportunities. Whether you are a manager, engineer, executive or a student, I invite you to experience the exciting developments in electronic components and technology during the 2013 ECTC. I also would like to take this opportunity to thank our sponsors, exhibitors, authors, speakers, instructors, session chairs, committee members, and arrangements, finance, publication, and publicity chairs, as well as all the volunteers for their support and hard work in making the 63rd ECTC a great success. I look forward to a great experience in exciting Las Vegas on May 28 - 31, 2013.
It’s Vegas again!
According to the previous statistics, every time ECTC was held in Las Vegas, it was always a big crowd. I believe the same trend will continue in 2013. For people who survived from 2012 (if you know what I mean), you deserve a big treat and should enjoy yourself as much as possible in Vegas. Thanks to the effort of ECTC Executive Committee, this year we have the conference venue set up at the magnificent Cosmopolitan. Undoubtedly everybody will have a good time at this modern and well-equipped hotel.

In addition to the great venue, we also have a very strong technical program this year, in particular, on the 3D/TSV topics. I am very pleased to note that the ECTC Program Committee improved the Advance Program and compiled a table of “Session Summary by Interest Areas.” This will be very helpful for the attendees to navigate themselves among interested topics and sessions. I would like to take this opportunity to thank the Program Committee members for their thoughtful planning and considerate arrangement.

As a common practice, there are a number of activities organized by CPMT within ECTC. In the evening of May 28, there will be a panel session on “LED for Solid-State Lighting.” This panel will discuss emerging LED packaging technologies and global market trends. On May 30, CPMT will sponsor a plenary luncheon and several important awards will be presented during the luncheon. In the evening on the same day, a CPMT seminar will be held right after the Gala Reception. This seminar will focus on “Advanced Low Loss Dielectric Materials for High Frequency and High Bandwidth Applications.” On behalf of the IEEE CPMT Society, I would like to invite all of you to attend these special events.

See you all there!
Ricky Lee
President, IEEE CPMT Society

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WELCOME FROM ECTC SPONSORING ORGANIZATION

Badges
Conference attendees MUST wear the official conference badge to be admitted to all training courses, sessions, meals, Technology Corner exhibits and all conference sponsored social functions.

Medical Services
For emergency medical services, locate any hotel phone, whether in your room or elsewhere in the hotel, and follow its directions for emergencies. Hotel “house” phones have been placed throughout the hotel and conference area for your convenience. If no phone can be located, please locate the nearest hotel staff or ECTC staff for assistance with your emergency. The closest available hotel staff person may be at the front desk.

Personal Property
The hotel’s safety deposit box is available for storing your valuables; particularly cash and jewelry. If there is a mini-safe in your room, you should consider using it.

Smoking Policy
The hotel allows smoking on its premises in designated smoking areas; however, smoking is NOT permitted at any ECTC activities including, but not limited to, functions, events, sessions, or seminars as well. Thank you for your consideration and cooperation.

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Corning® Semiconductor Glass Wafers
Enabling Next-Generation Glass Solutions For Advanced Packaging

CORNING

www.corning.com/semi/glass
Tuesday, May 28, 2013  
1:00PM - 6:00PM  
Condona, 2nd Floor

Since 1994, iNEMI (the International Electronics Manufacturing Initiative) has been developing a biennial technology roadmap spanning a 10-year horizon. Since 2011 iNEMI has been holding roadmapping meetings at ECTC. This year we will be holding an open meeting to prioritize the research needs identified in the 2013 Roadmap; the output will be the publication of the 2013 iNEMI Research Priorities.

Open to all conference attendees.
Registration
ECTC registration will be open at the ECTC Registration Desk located on the 4th floor in the Chelsea Commons Area.
Monday, May 27, 2013 – 3:00 p.m. - 5:00 p.m.
Tuesday, May 28, 2013 – 6:45 a.m. - 8:15 a.m.*
(AM PD Courses & Special Session Only)*
Tuesday, May 28, 2013 – 8:15 a.m. - 5:00 p.m.
(All conference attendees)
Wednesday, May 29, 2013 – 6:45 a.m. - 4:00 p.m.
Thursday, May 30, 2013 – 7:30 a.m. - 4:00 p.m.
Friday, May 31, 2013 – 7:30 a.m. - 12:00 p.m.
*The above schedule for Tuesday will be vigorously enforced to prevent students from being late for their courses. Please make sure to take advantage of the 6:45am start time on Tuesday, May 28 as registration becomes very congested prior to the start of morning Professional Development Courses.

Door Registration Fees
Door Registration with Proceedings on USB drive
IEEE Member Full Registration .................. $725
IEEE Member Speaker / Session Chair ........ $625
IEEE Member One Day ............................ $475
IEEE Member Speaker One Day ............... $350
Non-Member Full Registration ................. $870
Non-Member Speaker / Session Chair ...... $625
Non-Member One Day ............................ $475
Non-Member Speaker One Day ............... $350
Exhibit Booth Attendant ........................ $0

Student ........................................... $250
Student Speaker .................................. $250
Exhibits Only ..................................... $20

Tuesday Professional Development Courses
IEEE Members and Non-Members
Tuesday AM or PM Course with luncheon .... $475
Tuesday All-Day Courses with luncheon .... $675
Tuesday Student All-Day Courses with luncheon .... $125
Extra Luncheon Tickets for each day ........ $50
Extra Proceedings with registration .......... $100

Professional Development Course Instructors Breakfast
PDC Instructors and Proctors are required to attend a briefing breakfast.
6:45 a.m. Tuesday – PDC Instructors and Proctor Briefing
(Room Location: Chelsea 2)

Session Chairs and Speakers Breakfast
Session Chairs and speakers are requested to attend a complimentary continental breakfast on the morning of their sessions/presentations. At this time, presentations will be transferred to the conference PC, which is loaded with Windows XP and MS Office 2003.
7:00 a.m. Wednesday thru Friday
(Room Location: Chelsea 1)

Speaker Prep Room
Speakers should prepare and review their digital presentations as follows: 7:00 a.m. – 5:00 p.m., Tuesday – Friday (Room Location: Yaletown 3)
(It is extremely important to assure that your presentation, presentation software and computer work flawlessly with the digital projector provided.)

Luncheons

Tuesday, May 28, 2013
Noon (Chelsea 2)
The Electronic Components and Technology Conference will sponsor a luncheon for all Professional Development Courses attendees, proctors and PDC committee members.

Wednesday, May 29, 2013
Noon (Chelsea 1 & 5)
The Electronic Components and Technology Conference will sponsor a luncheon for conference attendees. Best and Outstanding Papers will be awarded. The guest speaker will be Chris Welty of IBM Corporation.

Thursday, May 30, 2013
Noon (Chelsea 1 & 5)
The IEEE Components, Packaging and Manufacturing Technology Society will sponsor a luncheon for conference attendees. The CPMT awards will be presented.

Friday, May 31, 2013
Noon (Chelsea 1 & 5)
The ECTC Program Chair will sponsor a luncheon for conference attendees.

There will be a raffle for attendees.
2013 SPECIAL SESSION
Tuesday, May 28, 2013
10:00 AM – Noon
Condesa 3, 2nd Floor
The Role of Wafer Foundries in Next Generation Packaging
Chair: Sam Karikalan, Broadcom Corporation
Speakers:
Jerry Tzou, TSMC
David McCann, GLOBALFOUNDRIES
Kurt Huang, UMC
Jon Casey, IBM Corporation
Herb Huang, SMIC

2013 ECTC PANEL SESSION
Tuesday, May 28, 2013
7:30 - 9:30 p.m.
Mont-Royal 1 & 2, 4th Floor
LED for Solid-State Lighting – For a Brighter Future
Chair: Ricky Lee, Hong Kong University of Science and Technology
Co-chair: Kouchi Zhang, TU Delft & Philips Lighting
Speakers:
Ling Wu, China Solid-State Lighting Alliance, China
Mark McClear, Cree Components, USA
Ron Bonne, Philips Lumileds, USA
Nils Erkamp, TNO, The Netherlands
Michael McLaughlin, Yole Development, USA

2013 ECTC PLENARY SESSION
Wednesday, May 29, 2013
7:00 - 9:00 p.m.
Mont-Royal 1 & 2, 4th Floor
Packaging Challenges Across the Wireless Market Supply Chain
Chair: Lou Nicholls, Amkor Technology
Speakers:
Timo Henttonen, Nokia
Steve Bezuk, Qualcomm Technologies, Inc.
Waite Warren, RFMD
Roger St. Amand, Amkor Technology
Soonjin Cho, SEMCO

2013 CPMT SEMINAR
Thursday, May 30, 2013
8:00 - 10:00 p.m.
Mont-Royal 1 & 2, 4th Floor
Advanced Low Loss Dielectric Materials for High Frequency and High Bandwidth Applications
Chair: Kishio Yokouchi, Fujitsu Interconnect Technologies Ltd.
Co-chair: Venky Sundaram, Georgia Institute of Technology
Speakers:
Yuya Suzuki, Zeon Corporation
Yasuyuki Mizuno, Tsukuba Research Laboratory, Hitachi Chemical Co., Ltd.
Shin Teraki, NAMICS Corporation
Hirohisa Narahashi, The Research Institute for Bioscience Products & Fine Chemicals, Ajinomoto Co., Inc.

2013 ECTC MODELING SESSION
Tuesday, May 28, 2013 • 2:00 - 4:30 p.m.
Condesa 3, 2nd Floor
Modeling and Simulation Challenges in 3D Systems
Chair: Yong Liu, Fairchild Semiconductor
Co-Chair: Dan Oh, Altera


A Comparative Simulation Study of 3D/Through Silicon Stack Assembly Processes, Kamal Karmanal – Cielution LLC
Thermo-Mechanical Challenges for Processing and Packaging Stacked Ultrathin Wafers, Mario Gonzalez, Bart Vandevelde, Antonio La Manna, Bart Swinnen, and Eric Beyne – IMEC

Keynote Speaker: Cloud-Based Scalable Electromagnetic Solvers for 3D Package Modeling, Vikram Jandhyala – University of Washington, Nimbl
Signal and Power Integrity Analysis of a 256GB/s Double-Sided IC Package with a Memory Controller and 3D Stacked DRAM, Wendem Beyene, Hai Lan, Scott Best, David Secker, Don Mullen, Ming Li, and Tom Giovanni – Rambus Inc.
Optimization of 3D Stack for Electrical and Thermal Integrity, Rishik Bazaz, Jianyong Xie, and Madhavan Swaminathan – Georgia Institute of Technology

These sessions/seminars are open to all conference attendees.
### Professional Development Courses

**Tuesday, May 28, 2013**

<table>
<thead>
<tr>
<th>Morning Courses 8:00 AM – 12:00 PM</th>
<th>Afternoon Courses 1:15 – 5:15 PM</th>
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<tr>
<td><strong>Yaletown 4</strong></td>
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<td><strong>Chelsea 5</strong></td>
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**Refreshment Breaks – 10:00 - 10:20 a.m. & 3:00 - 3:20 p.m.**
- Mont-Royal Commons & Chelsea Commons

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**ECTC Student Reception**

**Tuesday, May 28, 2013**
- **5:00 - 6:00 p.m.**
- **Room: Chelsea 2**
- **Host: Eric Perfecto – IBM Corporation**

Students, have you ever wondered how the ECTC technical committees review and select papers? Or, just what subjects, content and paper organization make a standout ECTC paper? Then please come to the ECTC Student Reception. You’ll have a chance to enjoy some good food and meet with representatives of each technical subcommittee. Don’t miss this chance for an inside view of technical subcommittee operations. Sponsored by the IBM Corporation.

**General Chair’s Speakers Reception**

**Tuesday, May 28, 2013**
- **6:00 - 7:00 p.m.**
- **Room: Blvd Pool North (Outside Pool Area, 4th floor, facing the Las Vegas Strip); Rain backup: Chelsea 2**

Invited session chairs and speakers are requested to attend this reception.

**Technology Corner Reception**

**Wednesday, May 29, 2013**
- **5:30 - 6:30 p.m.**
- **Room: Chelsea 3 & 4**

All attendees and guests are invited to attend this exhibitor sponsored reception. Please use this time to mix and mingle with all exhibitors, learn about their products and services, and pick up a few giveaways.

**63rd ECTC Gala Reception**

**Thursday, May 30, 2013**
- **6:30 p.m.**
- **Room: Chelsea 1 & 5**

All badged attendees and guests are invited to attend our Gala Reception. This is a great way to meet your conference colleagues, speakers, exhibitors, guests, and the ECTC Executive Committee.

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**Continuing Education Units**

The IEEE Components, Packaging and Manufacturing Technology Society (CPMT) has been authorized to offer Continuing Education Units (CEUs) by the International Association for Continuing Education and Training (IACET) for all Professional Development Courses that will be presented at the 63rd ECTC. CEUs are recognized by employers for continuing professional development as a formal measure of participation and attendance in “non-credit” self-study courses, tutorials, symposia and workshops. IEEE CPMT CEUs can be applied towards the “IEEE CPMT Professional Development Certificate.” Complete details, including voluntary enrollment forms, will be available at the conference. All costs associated with ECTC Professional Development Courses CEUs will be underwritten by the conference, i.e. there are no additional costs for Professional Development Courses attendees to obtain CEU credit.
**2012 ECTC PAPER AWARDS**

### Best of Conference Papers
The Electronic Components and Technology Conference is proud to announce the “Best of Conference” papers selected from the 62nd ECTC proceedings. The authors of the Best Session Paper share a check for US $2,500 and the authors of the Best Poster Paper share a check for US $1,500. The winning authors also receive a personalized plaque commemorating their achievement.

#### Best Session Paper
**(Session 28, paper 4)**
**Modeling and Reliability Characterization of Area-Array Electronics Subjected to High-G Mechanical Shock Up to 50,000G**
Pradeep Lall, Kewal Patel, Ryan Lowe, Mark Strickland, Jim Blanche, Dave Geist, Randall Montgomery – Auburn University

#### Best Poster Paper
**(Session 37, paper 17)**
**Void Formation during Reflow Soldering**

### Outstanding Papers
The winning authors for Conference Outstanding Session and Poster Papers receive a personalized plaque commemorating their achievement and will share a check for US $1,000.

#### Outstanding Session Paper
**(Session 24, paper 6)**
**A 77 GHz SiGe Single-Chip Four-Channel Transceiver Module with Integrated Antennas in Embedded Wafer-Level BGA Package**
M. Wojnowski, R. Lachner, J. Böck, G. Sommer, and K. Pressel – Infineon Technologies AG

#### Outstanding Poster Paper
**(Session 37, paper 11)**
**3D Stacked Microfluidic Cooling for High Performance 3D ICs**
Yue Zhang, Ashish Dembla, Yogendra Joshi, and Muhammad S. Bakir – Georgia Institute of Technology

### Intel Best Student Paper
The winning student receives a personalized plaque and a check for $2,500. The following paper was selected based on the Intel Best Student Paper competition conducted at the 62nd ECTC:

**(Session 34, Paper 4)**
**Interlayer Dielectric Cracking in Back End of Line (BEOL) Stack**
Sathyanarayanan Raghavan, Ilko Schmadlak and Suresh K. Sitaraman – Georgia Institute of Technology

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### COMMITTEE MEETINGS • ASSOCIATED COMMITTEE MEMBERS ONLY

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<tr>
<td>INEMI Meeting</td>
<td>CPMT Materials &amp; Processes TC</td>
<td>CPMT Photonics TC</td>
<td>ECTC Executive Committee</td>
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<td>8:00 a.m. – 5:00 p.m.</td>
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<td>ITRS Assemblies &amp; Packaging Technology Committee</td>
<td>CPMT High-Density Substrates &amp; Boards TC</td>
<td>CPMT RF &amp; THz Technologies TC</td>
<td>ECTC Governing/Executive Committee</td>
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<td>5:00 p.m. – 7:00 p.m.</td>
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<td>5:00 p.m. – 7:00 p.m.</td>
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<td>CPMT Region 8 Advisory Committee</td>
<td>CPMT Technical Committee Chairs</td>
<td>CPMT Thermal &amp; Mechanical TC</td>
<td>ECTC Governing/Executive Committee</td>
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<td>9:00 p.m. – 10:30 p.m.</td>
<td>6:00 p.m. – 7:00 p.m.</td>
<td>5:30 p.m. – 6:30 p.m.</td>
<td>Reception</td>
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<td>ECTC OPTO Committee</td>
<td>Program Subcommittee Chairs &amp; Assistent Chairs Reception</td>
<td>ECTC 2014 Program Committee Meeting</td>
<td>General Chair’s Suite</td>
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<td>9:00 p.m. – 10:30 p.m.</td>
<td>6:30 p.m. – 7:30 p.m.</td>
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<td>ECTC Interconnection Committee</td>
<td>ECTC Governing/Executive Committee</td>
<td>ECTC Governing/Executive Committee</td>
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<td>Yaletown 4, 4th floor</td>
<td>Condesa 6, 2nd floor</td>
<td>Reception</td>
<td>General Chair’s Suite</td>
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<td>Program Sessions: Wednesday, May 29, 8:00 a.m. - 11:40 a.m.</td>
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<td><strong>Session 1: 3D Assembly and Reliability</strong></td>
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<td>Committee: Advanced Packaging</td>
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<td>Mont-Royal 1</td>
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<td>Session Co-Chairs:</td>
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<td>John Knickerbocker – IBM Corporation</td>
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<td>Sam Karikalan – Broadcom Corporation</td>
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<tr>
<td>1. 8:00 a.m. – Reliability Studies on Micro-Bumps for 3D TSV Integration</td>
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<td>Ho-Young Son, Sung-Kwon Nah, Hyun-Hee Jung, Woong-Sun Lee, Jee-Sung Oh, and Nam-Seog Kim – SK Hynix Inc.</td>
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<td>2. 8:25 a.m. – Investigation on the Properties and Processibility of Polymeric Insulation Layers for Silicon Via</td>
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<td>3. 8:50 a.m. – TSV and Cu-Cu Direct Bond Wafer and Package-Level Reliability</td>
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<td>4. 10:00 a.m. – Analyzing the Behavior and Shear Strength of Common Adhesives Used in Temporary Bonding</td>
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<td>J.A. Sharpe, M.B. Jordan, S.L. Burkett, and M.E. Barkey – University of Alabama</td>
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<td>6. 10:50 a.m. – Low Cost, Room Temperature Debondable Spin-On Temporary Bonding Solution: A Key Enabler for 2.5D/3D IC Packaging</td>
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<td>Ranjith S.E. John, Herman Meynen, Sheng Wang, Peng-Fei Fu, Craig Yeakle, Sang Wook W. Kim, and Lyndon J. Larson – Dow Corning Corporation; Scott Sullivan – Suss MicroTec</td>
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<td>7. 11:15 a.m. – Assembly of 3D Chip Stack with 30um-Pitch Micro Interconnects Using Novel Arrayed-Particles Anisotropic Conductive Film</td>
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<td><strong>Session 2: 3D Materials and Processing</strong></td>
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<td>Committee: Materials &amp; Processing</td>
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<td>Session Co-Chairs:</td>
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<td>Mikel Miller – Draper Laboratory</td>
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<td>Bing Dang – IBM Corporation</td>
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<tr>
<td>1. 8:00 a.m. – Development of 3D Through Silicon Stack (TSS) Assembly for Wide IO Memory to Logic Devices Integration</td>
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<td>2. 8:25 a.m. – Reliability Evaluation of a CoWoS-Enabled 3D IC Package</td>
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<td>3. 8:50 a.m. – Process Integration of 3D Si Interposer with Double-Sided Active Chip Attachments</td>
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<td>4. 10:00 a.m. – Ultra-Fine Trench Circuit on Polymer Film</td>
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<td>Takaharu Honda, Yoosuke Nitta, Kei Nakamura, Hirooki Hirano, Masanobu Saruta, Toshiki Inoue, and Osamu Nakao – Fujikura, Ltd.</td>
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<td>5. 10:25 a.m. – WSS and ZoneBOND Temporary Bonding Techniques Comparison for 80µm and 55µm Functional Interposer Creation</td>
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<td>6. 10:50 a.m. – Low Cost, Room Temperature Debondable Spin-On Temporary Bonding Solution: A Key Enabler for 2.5D/3D IC Packaging</td>
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<td>Ranjith S.E. John, Herman Meynen, Sheng Wang, Peng-Fei Fu, Craig Yeakle, Sang Wook W. Kim, and Lyndon J. Larson – Dow Corning Corporation; Scott Sullivan – Suss MicroTec</td>
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<td>7. 11:15 a.m. – Carbon Nanotube Array as High Impedance Interconnects for Sensing Device Application</td>
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<td>Dunlin Tan and Dominique BAillarguet – CINTRA; Chin Chong Yap and Beng Kang Tay – Nanyang Technological University; David Hse, Jang Jun Yu, Jean-Luc Reverchon, and Philippe Boit – Thales</td>
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<td><strong>Session 3: Novel Interconnections</strong></td>
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<td>Committee: Interconnections</td>
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<td>Session Co-Chairs:</td>
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<td>James E. Morris – Portland State University</td>
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<td>Lei Shan – IBM Corporation</td>
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<tr>
<td>1. 8:00 a.m. – Effects of Nanofiber Materials of Nanofiber Anisotropic Conductive Adhesives (Nanofiber ACA) for Ultra-Fine Pitch Electronic Assemblies</td>
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<td>Kyoung-Lim Suk and Kyung-Wook Pak – KAIST</td>
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<td>2. 8:25 a.m. – A Novel Non-TSV Approach to Enhancing the Bandwidth in 3-D Packages for Processor-Memory Modules</td>
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<td>Dev Gupta – APSTL</td>
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<td>3. 8:50 a.m. – Three-Path Electroplated Copper Compliant Interconnects – Fabrication and Modeling Studies</td>
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<td>Raphael Okerere and Suresh K. Sitaraman – Georgia Institute of Technology</td>
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**Refreshment Break: 9:15 a.m. – 10:00 a.m. (Chelsea 3 & 4)**
### Program Sessions: Wednesday, May 29, 8:00 a.m. - 11:40 a.m.

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<th>Session 5: New Directions in Packaging</th>
<th>Session 6: Optical Interconnects</th>
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<td>Session Co-Chairs:</td>
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<tr>
<td>John H. L. Pang – Nanyang Technological University</td>
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<td>Deepak Goyal – Intel Corporation</td>
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<tr>
<td>1. 8:00 a.m. – Define Electrical Packing</td>
<td>1. 8:00 a.m. – Optical Backplane for Board-to-Board Interconnection Based on a Glass Panel Gradient-Index Multimode Waveguide Technology</td>
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<td>Temperature Cycling Requirement with Field Measured User Behavior Data</td>
<td>Lars Brusberg, Henning Schröder, and Julia Roder – Fraunhofer IZM; Richard Petrow and Allen Miller – Xyratex Technology Ltd; Simon Whalley – ILFA Testtechnologie GmbH; Christian Herbst, Marcel Neitz, and Klaus-Dieter Lang – TU Berlin</td>
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<tr>
<td>Min Pei, Ru Han, Daesol Kwon, Alan Luceiro, Vasu Vasudevan, Robert Kwasnick, and Praveen S. Polasam – Intel Corporation</td>
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<td>2. 8:25 a.m. – Characterization of Aging Effects in Lead-Free Solder Joints using Nanoindentation</td>
<td>2. 8:25 a.m. – Single-Chip 4TX + 4RX Optical Module Based on Holey SiGe Transceiver IC</td>
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<td>3. 8:50 a.m. – Effects of Reliability Testing Methods on Microstructure and Strength at the Cu Wire-Al Pad Interface</td>
<td>3. 8:50 a.m. – FPC-Based Compact 25-Gb/s Optical Transceiver Module for Optical Interconnect Utilizing Novel High-Speed FPC Connector</td>
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<td>4. 10:00 a.m. – Use of RF-Based Technique as a Metrology Tool for TSV Reliability Analysis</td>
<td>4. 10:00 a.m. – Optical Packaging of Silicon Photonic Devices for External Connection of Parallel Optical Signals</td>
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<td>Chulwuk Okoro, Pavel Kabos, Jan Obrzut, and Yow S. Oberg – NIST; Klaus Hummel – SEMATECH</td>
<td>Yoshihisa Taira and Hidetoshi Numata – IBM Corporation</td>
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<tr>
<td>5. 10:25 a.m. – On the Use of High Precision Electrical Resistance Measurement for Analyzing the Damage Test of Pb-Free Solder Interconnects</td>
<td>5. 10:25 a.m. – Modeling, Design, and Fabrication of Ultra-High Bandwidth 3D Glass Photonics (3DGP) in Glass Interposers</td>
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<tr>
<td>6. 10:50 a.m. – Unique Adhesion Testing and MSL Modeling</td>
<td>6. 10:50 a.m. – Assembly Development of 1.3 Tbi/s Full Duplex Optical Module</td>
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<tr>
<td>Masazumi Amagi and Kentaro Takao – Texas Instruments</td>
<td>Yeshoshu Benjamin, Kobi Hasharoni, and Michael Mesh – Compass Electro Optical Systems</td>
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<td>7. 11:15 a.m. – Acoustic Emission Detection of BGA Components in Spherical Bend</td>
<td>7. 11:15 a.m. – Low-Loss Design and Fabrication of Multimode Polymer Optical Waveguide Circuit with Crossings for High-Density Optical PCB</td>
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**Refreshment Break: 9:15 a.m. – 10:00 a.m. (Chelsea 3 & 4)**
Program Sessions: Wednesday, May 29, 1:30 p.m. - 5:10 p.m.

Session 7: Interposers

Committee: Advanced Packaging
Mont-Royal 1
Session Co-Chairs:
Subhash L. Shinde – Sandia National Laboratory
Peter Ramm – Fraunhofer EMFT

1. 1:30 p.m. – Full Integration of a 3D Demonstrator with TSV First Interposer, Ultra Thin Die Stacking, and Wafer Level Packaging

2. 1:55 p.m. – Fabrication and Testing of Thin Interposers with Multilevel Frontside and Backside Metallization and Co-Filled TSVs

3. 2:20 p.m. – Interposer Technology for High Bandwidth Interconnection Applications

4. 3:00 p.m. – Package Demonstration of Interposer with Integrated TSVs and Flexible Compliant Interconnects
Ivan Shubin, Alex Chow, Hirien Thacker, Kaman Raj, Ashok Krishnamoorthy, James Mitchell, and John Cunningham – Oracle; Eugene Chow and Dirk DeBruyker – Palo Alto Research Center (PARC); Koji Fujimoto – Dai Nippon Printing Co., Ltd.

5. 3:30 p.m. – Electrical and Morphological Characterization for High Integrated Silicon Interposer and Technology Transfer from 200mm to 300mm Wafer

6. 4:00 p.m. – Demonstration of Low Cost, High Performance, and High Reliability of 2.5D Poly crystalline Silicon Interposer with Fine Pitch Through Vias, Redistribution Layers, and Cu Microbump Interconnections
Venky Sundaram, Qiao Chen, Tao Wang, Hao Lu, Yuya Suzuki, Raj Pulkurthi, and Rao Tummala – Georgia Institute of Technology

7. 4:45 p.m. – Development of Through Glass Via (TGV) Formation Technology Using Electrical Discharging for 2.5D/3D Integrated Packaging
Shintaro Tahashiti, Kohei Horisuchi, Kentaro Tatsukashi, Motoaki Ono, and Nobuhiyo Imajo – Asahi Glass Company, Ltd.; Tim Mobely – Mode Solutions, Inc.

Session 8: 3D Reliability and Packaging Challenges

Committee: Applied Reliability
Mont-Royal 2
Session Co-Chairs:
Toni Mattila – Aalto University
Jeffrey Suhling – Auburn University

1. 1:30 p.m. – Thermomechanical and Electromechanical Reliability of Fine-Pitch Through-Package-Copper Vias (TPV) in Thin Glass Interposers and Packages
Kaya Demir, Koushik Ramachandran, Qiao Chen, Vijay Sukumar, Raghu Pucha, Venka kne Sundaram, and Rao Tummala – Georgia Institute of Technology; Yoshio Sato – Asahi Glass Co., Ltd.

2. 1:55 p.m. – Impacts of Static and Dynamic Local Bending of Thinned Si Chip on MOSFET Performance in 3-D Stacked LSI

3. 2:20 p.m. – Reliability Characterization of Chip-on-Wafer-on-Substrate (CoWoS) 3D IC Integration Technology
Larry Lin, Tung-Chin Yeh, Jun-Lin Wu, Gary Lu, Tsung-Fu Tsai, Larry Chen, and An-Tai Xu – Taiwan Semiconductor Manufacturing Company, Ltd.

4. 3:00 p.m. – Accelerated Reliability Testing and Modeling of Cu-Plated Through Encapsulant Vias (TEVs) for 3D-Integration
B. Wunderle, Jens Heilmann, and Sridhar Ganesh Kumar – TU Chemnitz; Ole Hoeckl – TU Chemnitz, Fraunhofer IZM; Hans Walter, Olaf Wüster, Gunter Engelmann, and M. Jüngen; Wolf – Fraunhofer IZM; Gottfried Beer and Klaus Pressel – Infineon Technologies AG

5. 3:30 p.m. – Study of Large Silicon Interposers Report on Board

6. 4:00 p.m. – Demonstration of Low Cost, High Performance, and High Reliability of 2.5D Poly crystalline Silicon Interposer with Fine Pitch Through Vias, Redistribution Layers, and Cu Microbump Interconnections
Venky Sundaram, Qiao Chen, Tao Wang, Hao Lu, Yuya Suzuki, Raj Pulkurthi, and Rao Tummala – Georgia Institute of Technology

7. 4:45 p.m. – Extension of Micro-Raman Spectroscopy for Full-Component Stress Characterization of TSV Structures
Qiu Zhao, J. Jin, R. Huang, and P.S. Ho – University of Texas, Austin

Session 9: Advanced Flip Chip Technologies

Committee: Interconnections
Nolita 1
Session Co-Chairs:
Lou Nichols – Armos Technology Inc.
William Chen – Advanced Semiconductor Engineering Inc.

1. 1:30 p.m. – Challenges of Chip-to-Package Interaction for 22nm Technology with Ultra Low k and Pb-Free Interconnects
Chris Muzzy, Richard Bisson, John Cincotta, Danielle Degraw, Edward Engbrecht, Jason Gill, Naftali Lustig, Karen McAulhagh, Sylvain Ouimet, Joseph Ross, and David Turnbull – IBM Corporation

2. 1:55 p.m. – Ultra-Thin and Ultra-High I/O Density Package-on-Package (3D Thin PoP) for High Bandwidth of Smart Systems
Song Jin Kim, Chimay Honraoa, P. Markondeya Raj, Venky Sundaram, and Rao Tummala – Georgia Institute of Technology

3. 2:20 p.m. – A PoP Structure to Support I/O over 1000
Dy-Chung Hu, Chun-Ting Lin, and Ying-Chih Chan – Unimicron Technology Corporation

Refresher Breaks: 2:45 p.m. - 3:30 p.m. (Chelsea 3 & 4)
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<th>Session 11: Biomedical Electronics</th>
<th>Session 12: High Brightness LEDs and Material</th>
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<tr>
<td>Shawn Shi – Medtronic Corporation</td>
<td>C. S. Premachandran – GLOBALFOUNDRIES</td>
<td>Henning Schroeder – Fraunhofer IZM</td>
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1. **1:30 p.m.** – Strip Warpage Analysis of a Flip Chip Package Considering the Mould Compound Processing Parameters
   Eric Quyang and MyoungSu Chae – STATS ChipPAC, Ltd.

2. **1:55 p.m.** – Thermoplastic Based System-in-Package for RFID Application
   Christine Kalnaymer, Barbara Pahl, and Arian Grams – Fraunhofer IZM; Joao Marques and Klaus-Dieter Lang – TU Berlin; Thomas Szwald – NXP Semiconductors

3. **2:20 p.m.** – 3D Printing of Structures with Embedded Circuit Boards Using Novel Holographic Optics
   Shuai Hou and John Tyrer – Loughborough University

4. **3:30 p.m.** – Low Temperature Fine Pitch Flex-on-Flex (FOF) Assembly Using Nanofiber Sn58Bi Solder Anisotropic Conductive Films (ACFs) and Ultrasonic Bonding Method
   Tae Wan Kim, Kyoung-Lim Suk, and Kyung-Wook Paik – KAIST

5. **3:55 p.m.** – Effective Voiding Control of QFN Via Solder Mask Patternning
   Derrick Herron, Yan Liu, and Ning-Cheng Lee – Indium Corporation

6. **4:20 p.m.** – Warpage Analysis and Improvement for a Power Module
   Yang Liu, Yunmin Liu, Zhongfa Yuan, Tyler Chen, Keunhyuk Lee, and Suresh Belani – Fairchild Semiconductor Corporation

7. **4:45 p.m.** – Solder Joint Properties of Sn-Ag-Cu Solders on Environmental-Friendly Plasma Surface Finish
   Sang-Hyun Kwon, Kyeong-Ho Kim, Won-II Seo, Chang-Woo Lee, and Sehoon Yoo – Korea Institute of Industrial Technology (KITECH); Nam-Sun Park – Jejung Hankook Ltd; Young-Bae Park – Andong National University

8. **4:45 p.m.** – Quasi-Conformal Phosphor Dispensing on LED for White Light Illumination
   S.W. Ricky Lee, Xungao Guo, Dac yuan Niu, and Jeffery C.C. Lo – Hong Kong University of Science & Technology

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<th>Refreshment Break: 2:45 p.m. - 3:30 p.m. (Chelsea 3 &amp; 4)</th>
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1. **1:30 p.m.** – Smart Flexible Planar Electrodes for Electrochemotherapy and Biosensing
   Paolo Nenzu, Agnese Derazi, Konstantin Kholostov, Rocco Crescenzi, Francesca Apolonia, Micaela Liberti, Paolo Marraccino, Ruggero Cadossi, and Marco Balucani – University of Rome; Alessia Ongaro – University of Ferrara

2. **1:55 p.m.** – Flexible, Transparent Electronics for Biomedical Applications
   Michael KlopfenGP. Li, and Mark Bachman – University of California, Irvine; Chris Contorner, Koutaku Inoue, and Hideo Honma – Kanto Gakuin University

3. **2:20 p.m.** – Epidermal Electronics for Seamless Monitoring of Biopotential Signals
   Mitsu Daidon, Conrad Rafferty, Yuan-Hu Hsu, Henry Wei, Kevin Dowling, Brina Mowery, Greg Levesque, Gil Huppert, Brian Elolampi, and Dan Davis – mClO, Inc.

4. **3:30 p.m.** – Sensor Integrated Microfluidics for Compact Micro-Reactors
   Erik Jung, Martin Biehrens, Victoria Schulte, and Moritz Hubl – Fraunhofer IZM; Leopold Georg and Klaus-Dieter Lang – TU Berlin

5. **3:55 p.m.** – 3-Axis MEMS Accelerometer-Based Implantable Heart Monitoring System with Novel Fixation Method


7. **4:45 p.m.** – Very High Power Density LED Modules on Aluminum Substrates with Embedded Water Cooling
   Marc Schneider, Benjamin Leyerer, Christian Herbold, and Stefan Maikowske – Karlsruhe Institute of Technology

8. **5:10 p.m.** – High Refractive Index and Transparency Nanocomposites as Encapsulant for High Brightness LED Packaging
   Yan Liu, Ziyn Lin, Xueyong Zhao, and Kyoung-Sik Moon – Georgia Institute of Technology; Sehoon Yoo – Korea Institute of Industrial Technology; Ji Choi – El Lighting Co.; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong
**Program Sessions: Thursday, May 30, 8:00 a.m. - 11:40 a.m.**

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<th>Session 15: Enabling Technologies for Flip Chip Assembly</th>
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<td>Mont-Royal 2</td>
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<td><strong>Session Co-Chairs:</strong></td>
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<tr>
<td>Christopher Bower – Semprius, Inc.</td>
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<td>Erik Jung – Fraunhofer IZM</td>
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<td><strong>Program Sessions:</strong></td>
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<tr>
<td>1. 8:00 a.m. – TSV Last for Hybrid Pixel Detectors: Application to Particle Physics and Imaging Experiments</td>
<td>1. 8:00 a.m. – Model for Prediction of Package-on-Package Warpage and the Effect of Process and Material Parameters</td>
<td>1. 8:00 a.m. – Low-k ILD Reliability through Package-Assembly Engineering Appropriate Stress Tests and Process Certification Criteria</td>
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<td>2. 8:25 a.m. – Dielectric Stack Engineering for Via-Reveal Passivation</td>
<td>2. 8:25 a.m. – Design for Reliability of Multi-Layer Thin Film Stretchable Interconnects</td>
<td>2. 8:25 a.m. – Flip Chip Assembly Method Employing Differential Heating/cooling for Large Dies with Coreless Substrates</td>
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<td>3. 8:50 a.m. – Low-Cost Micrometer-Scale Silicon Vias (SVs) Fabrication by Metal-Assisted Chemical Etching (MaCE) and Carbon Nanotubes (CNTs) Filling</td>
<td>3. 8:50 a.m. – A More Practical Method of Predicting Flip Chip Solder Bump Electromigration Reliability</td>
<td>3. 8:50 a.m. – 3D Integration of CMOS Image Sensor with Co-Processor Using TSV Last and Micro-Bumps Technologies</td>
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<td>4. 10:00 a.m. – Impact of Post-Plating Anneal and Through-Silicon Via Dimensions on Cu Pumping</td>
<td>4. 10:00 a.m. – Improvement of the Reliability of TSV Interconnections by Controlling the Crystallinity of Electroplated Copper Thin Films</td>
<td>4. 10:00 a.m. – Methodology to Evaluate Pre-Applied Underfill Materials with Concurrent Flux Capability for Ultra-Fine Pitch Solder-Based Interconnects</td>
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<td>5. 10:25 a.m. – A Quick-Turn 3D Structured ASIC Platform for Cost-Sensitive Dies</td>
<td>5. 10:25 a.m. – Characterization of Plasticity and Stresses in TSV Structures in Stacked Dies using Synchrotron X-Ray Microdiffraction</td>
<td>5. 10:25 a.m. – No Clean Flux Technology for Large Die Flip Chip Packages</td>
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<td>6. 10:50 a.m. – TSV-Based Quartz Crystal Resonator Using 3D Integration and Si Packaging Technologies</td>
<td>6. 10:50 a.m. – X-Ray Micro-Beam Diffraction Determination of Full-Stress Tensors in Cu TSVs</td>
<td>6. 10:50 a.m. – Ultra Large System-in-Package (SiP) Module and Novel Packaging Solution for Networking Applications</td>
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<td>7. 11:15 a.m. – Total Cost Effective Scallop Free Si Etching for 2.5D &amp; 3D TSV Fabrication Technologies in 300mm Wafer</td>
<td>7. 11:15 a.m. – Effect of Metal Finishing Fabricated by Electro and Electroless Plating Process on Reliability Performance of 30um-Pitch Solder Micro Bump Interconnection</td>
<td>7. 11:15 a.m. – Low-Cost E-Band Flip-Chip Assembly and Materials</td>
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<th>Session 17: Adhesives and Underfill Materials</th>
<th>Session 18: Thermal and Mechanical Modeling &amp; Simulation</th>
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<tr>
<td>Vikas Gupta – Texas Instruments</td>
<td>Stephanie Potisek – Dow Chemical</td>
<td>Erdogan Madenci – University of Arizona</td>
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<td><strong>1. 8:00 a.m. – Electromigration of Solder Balls for Wafer-Level Packaging with Different Under Bump Metallurgy and Redistribution Layer Thickness</strong></td>
<td><strong>1. 8:00 a.m. – Innovative Wafer-Level Encapsulation &amp; Underfill Material for Silicon Interposer Application</strong></td>
<td><strong>1. 8:00 a.m. – Modeling and Experimental Study of Thin Bond Line Thermal Interface Material Failure</strong></td>
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<td><strong>2. 8:25 a.m. – Electromigration Reliability and Current Carrying Capacity of Various WL CSP Interconnect Structures</strong></td>
<td><strong>2. 8:25 a.m. – Wafer Level Underfill Entrapment in Solder Joint During Thermocompression: Simulation and Experimental Validation</strong></td>
<td><strong>2. 8:25 a.m. – 3D vs 2D Modeling of the Effect of Die Size on Delamination in Encapsulated IC Packages</strong></td>
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<td><strong>3. 8:50 a.m. – Reliability Modeling and Testing of Advanced QFN Packages</strong></td>
<td><strong>3. 8:50 a.m. – Novel Surface Modification of Nanosilica for Low Stress Underfill</strong></td>
<td><strong>3. 8:50 a.m. – Effective Package-On-Package Warpage DOE Design with Analytical Method</strong></td>
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<tr>
<td>Li Li – Cisco Systems, Inc.</td>
<td>Ziyin Lin, Yan Liu, and Kyung-Sik Moon – Georgia Institute of Technology; C.P. Wong – Georgia Institute of Technology, Chinese University of Hong Kong</td>
<td>Shengmin Wen and Wei Lin – Amkor Technology</td>
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<td><strong>4. 10:00 a.m. – An Improved Model for Predicting Fatigue-Crack Propagation Behaviors in Multiple Solder Bumps on a BGA Package</strong></td>
<td><strong>4. 10:00 a.m. – The Optimization of the Composition of Non-Conductive Film and the Lamination to Wafer</strong></td>
<td><strong>4. 10:00 a.m. – Damage Pre-Cursor Based Assessment of Impact of High Temperature Storage on Reliability of Leadfree Electronics</strong></td>
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<td><strong>5. 10:25 a.m. – Grain Structure Evolution and Its Impact on the Fatigue Reliability of Lead-Free Solder Joints in BGA Packaging Assembly</strong></td>
<td><strong>5. 10:25 a.m. – Development of Highly Reliable Flip-Chip Bonding Technology Using Non-Conductive Adhesives (NCAs) for 20 µm Pitch Application</strong></td>
<td><strong>5. 10:25 a.m. – A Preliminary Solder Joint Life Prediction Model by Experiment and Simulation for Translation of Use Condition to Temperature Cycling Test Condition</strong></td>
</tr>
<tr>
<td>Hui Xu and Choong-Un Kim – University of Texas, Arlington; Tae-Kyu Lee – Cisco Systems, Inc.</td>
<td>Sun-Chul Kim, Myung-Hwan Hong, Ji-Hyun Lee, and Young-Ho Kim – Hanyang University</td>
<td>Ru Han, Min Pei, Alan Lucera, Daed Kwon, Yun Ge, Richard Harries, Pardeep Bhati, and Teyu Zheng – Intel Corporation</td>
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<td><strong>6. 10:50 a.m. – Failure Analysis of Thermally and Mechanically Stressed Plastic Core Solder Balls</strong></td>
<td><strong>6. 10:50 a.m. – High Thermal Conductive Adhesive Film for Cu and Al Plate Adhesion in Power Electronics Package</strong></td>
<td><strong>6. 10:50 a.m. – Use of Compliant Interconnects for Drop Impact Isolation</strong></td>
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<td><strong>7. 11:15 a.m. – An Eco-Friendly Cu-Zn Wetting Layer for Highly Reliable Solder Joints</strong></td>
<td><strong>7. 11:15 a.m. – The Effect of Coating Thickness on the Electrical Performance of Novel Isotropic Conductive Adhesives Prepared Using Metallised Polymer Micro-Spheres</strong></td>
<td><strong>7. 11:15 a.m. – Prediction of Board-Level Performance of WL CSP</strong></td>
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<td>Program Sessions: Thursday, May 30, 1:30 p.m. - 5:10 p.m.</td>
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<td><strong>Session 19: Interposer Characterization</strong></td>
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<td>Session Co-Chairs:</td>
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<tr>
<td>Matthew Yao – Rockwell Collins</td>
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<tr>
<td>Katsuyuki Sakuma – IBM Corporation</td>
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<tr>
<td>1. 1:30 p.m. – High Speed Signaling</td>
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<tr>
<td>Performance of Multilevel Wiring on Glass Substrates</td>
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<td>for 2.5D Integrated Circuit and Optoelectronic Integration</td>
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<tr>
<td>Xiaoqiong Gu, Renato Rimolo-Donadio, Russell Budd,</td>
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<td>Christian Baks, Lavanya Turtipati, Christopher Johnnes,</td>
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<tr>
<td>Daniel M. Kuchta, Clint L. Schow, and Frank Litach – IBM</td>
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<td>Corporation</td>
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</tbody>
</table>

| **Session 20: Challenges in 3D Integration**             |
| Committee: Assembly & Manufacturing Technology           |
| Mont-Royal 2                                            |
| Session Co-Chairs:                                       |
| Andy Tseng – Advanced Semiconductor Engineering, Inc.;  |
| Wei Koh – Pacrim Technology                             |
| 1. 1:30 p.m. – Flux-Assisted Self-Assembly with          |
| Microfluid Bonding Integration for 3D Heterogeneous       |
| Integration                                              |
| Yuka Ito – Tohoku University, Sumitomo Bakelite Co.,     |
| Ltd.; Takakuni Fukushima, Kang-Wook Lee, Tetsu Tanaka,   |
| and Masumasa Kayanagi – Tohoku University; Koji Choki    |
| – Sumitomo Bakelite Co., Ltd.                           |

| **Session 21: Advanced Substrate and Flip Chip Packaging**|
| Committee: Advanced Packaging                           |
| Nolita 1                                                |
| Session Co-Chairs:                                       |
| Young-Gon Kim – IDT                                      |
| Raj M. Master – Microsoft Corporation                   |
| 1. 1:30 p.m. – Nano-Silica Composite Laminate           |
| Katsura Hayashi, Tadashi Nagasawa, Keisaku Matsumoto,    |
| and Shinya Kawai – Kyocera Corporation                  |

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<th>Refreshment Breaks: 2:45 p.m. - 3:30 p.m. (Chelsea 3 &amp; 4)</th>
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<tr>
<td>4. 3:30 p.m. – Thermally Enhanced Pre-Applied Underfills</td>
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<td>for 3D Integration</td>
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<tr>
<td>Akihito Honke, Kazuki Okamoto, Hiroki Mori, and</td>
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<tr>
<td>Yasumitsu Otsu – IBM Corporation; Kohichiro Kawate,</td>
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<tr>
<td>Yorinobu Takamatsu, and Hiroko Aoyama – Sumitomo</td>
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<tr>
<td>3M, Ltd.</td>
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</table>

| 5. 3:55 p.m. – Integration Challenges of TSV              |
| Backside Via Reveal Process                               |
| Bo Kai Huang, Chien Ming Lin, Shin Jiang Huang, Ching     |
| Wen Chiang, Pin Cheng Huang, Guang Xin Chen, Chun         |
| Cheh Chao, and Chun Hung Lu – Siliconware Precision       |
| Industries Co., Ltd.                                      |

| 6. 4:20 p.m. – Mechanical and Board Level                |
| Reliability Considerations of Lidless Flip Chip          |
| BGA Packaging                                            |
| Shin Low, Inderjit Singh, Ganesh Harhanar, Laurene Yp,    |
| and Naol Zohri – Xilinx, Inc.; Mulugueta Abetik, Gowri    |
| Shankar Solisippan, Vineeth Vair, and Shane Lewis –     |
| Sanmina-SCI Corp.                                         |

| 7. 4:45 p.m. – Development and Characterization of a     |
| Through-Multilayer TSV Integrated SRAM Module             |
| Yunfui Zhu, Xin Sun, Runfeng Fang, Xiao Zhang, Yuan Bian, |
| Meng Chen, Jing Chen, Wengao Lu, and Yufeng Jin –        |
| Peking Univ.; Shenglin Ma – Xiamen Univ, Peking Univ.;   |
| Min Mao – Peking Univ, Beijing Information Science and    |
| Technology Univ.                                         |

| 8. 4:45 p.m. – Package-on-Package with Very Fine          |
| Pitch Interconnects for High Bandwidth                    |
| Ilyas Mohammed, Reynaldo Co, and Rajesh Katkar –         |
| Invensas Corporation                                       |

| 9. 4:45 p.m. – Development and Characterization of a      |
| Through-Multilayer TSV Integrated SRAM Module             |
| Min-Su Kim – University of Science & Technology, Korea    |
| Institute of Industrial Technology (KITECH); Yong-Ho Ko  |
| – Korea Institute of Industrial Technology (KITECH),      |
| KAIST, Sehoon Yoo and Chang-Woo Lee – Korea Institute of  |
| Industrial Technology (KITECH)                            |
|-----------------------------------------------|-------------------------------|----------------------------------|
| **Committee:** Applied Reliability            | **Committee:** Materials & Processing | **Committee:** Modeling & Simulation |
| Nolita 2                                      | Nolita 3                        | Yaletown 4                        |
| Session Co-Chairs:                            | Session Co-Chairs:              | Session Co-Chairs:                |
| Dongming He – Qualcomm Technologies, Inc.     | Yoichi Taira – IBM Japan        | Kernal Aygun – Intel Corporation  |
| 1. 1:30 p.m. – Reliability and Failure Mechanism of Solder Joints in Thermal Cycling Tests | 1. 1:30 p.m. – Reduced Graphene Oxide Based Schottky Diode on Flex Substrate for Microwave Circuit Applications | 1. 1:30 p.m. – Simultaneous Switching Noise Model by Distributed Power Port and Ground Current Capture |
| 2. 1:55 p.m. – Correlation of Reliability Models Including Aging Effects with Thermal Cycling Reliability Data | 2. 1:55 p.m. – Ultra-Thin, Self-Healing Decoupling Capacitors on Thin Glass Interposers Using High Surface Area Electrodes | 2. 1:55 p.m. – System Level Signal and Power Integrity Analysis for 3200Mbps DDR4 Interface |
| Jeffrey C. Suhling, Mohammad Motolah, Mohmad Mustafa, Jiwae Zhang, John L. Evans, Michael J. Bozack, and Pradeep Lall – Auburn University | Parthasarathi Chakraborti, Himani Sharma, P. Markondeya Raj, and Rao Tummala – Georgia Institute of Technology | June Feng, Bipin Dhara, Janani Chandrasekar, Yuri Trestakow, and Dan Oh – Altera Corporation |
| 3. 2:20 p.m. – Comparison of IMC Growth in Flip-Chip Assemblies with 100- and 200-µm-Pitch SAC305 Solder Joints | 3. 2:20 p.m. – Electrochemical Assembly of SAM on Copper for Epoxy/Copper Adhesion Improvement | 3. 2:20 p.m. – Analysis of Power Integrity and Its Jitter Impact in a 4.3Gbps Low-Power Memory Interface |
| Ye Tian – Huazhong University of Science and Technology, Georgia Institute of Technology; Xi Liu, Justin Chow, and Suresh K. Sitaraman – Georgia Institute of Technology; Yi Peng Wu – Huazhong University of Science and Technology | Stephen C.T.Kwok and Matthew M.F.Zien – Hong Kong University of Science & Technology | Hai Lan, Xinhai Jang, and Jihong Ren – Rambus, Inc. |
|        | 4. 3:30 p.m. – Chip-Side-Healing as a Basis for Robust Bare-Chip Assemblies | 4. 3:30 p.m. – Unconditionally Stable Explicit Method for the Fast 3D Simulation of On-Chip Power Distribution Network |
|        | Matthias Steurer and Jurgen Wilde – University of Freiburg | Tatatsuki Sekine and Hideki Asai – Shizuoka University |
|        | 5. 3:55 p.m. – Plastic Deformation Effect on Sn Whisker Growth in Electroplated Sn and Sn-Ag Solders | 5. 3:55 p.m. – Power Delivery Network Analysis of 3D Double-Side Glass Interposers for High Bandwidth Applications |
|        | 6. 4:20 p.m. – Effect of NCFs with Zn-Nanoparticles on the Interfacial Reactions of 40 um Pitch Cu Pillar/ Sn-Ag Bump for TSV Interconnection | 6. 4:20 p.m. – Development of Low Temperature Sintered Nano Silver Pastes Using MO Technology and Resin Reinforcing Technology |
|        | 7. 4:45 p.m. – Advanced In Situ Characterization of TIM1 Reliability | 7. 4:45 p.m. – Fast Voltage Drop Modeling of Power Grid with Application to Silicon Interposer Analysis |
|        | Peng Li, Yongmei Liu, Alfred La Mar, and Deepak Goyal – Intel Corporation | En-Xiao Liu and Er-Ping Li – Institute of High Performance Computing, A*STAR |
|        | 7. 4:45 p.m. – Facile Synthesis of BaTiO₃ Nanorods and Their Shape Effects on the Dielectric Constants of Polymer Composites | 7. 4:45 p.m. – Power Delivery Modeling for 3D Systems with Non-Uniform TSV Distribution |
|        | Pengli Zhu and Rong Sun – Chinese Academy of Science; C.P.Wong – Chinese University of Hong Kong | Huanyu He and Jian-Qiang Lu – Rensselaer Polytechnic Institute; Zheng Xu and Xiaoxiong Gu – IBM Corporation |
## Program Sessions: Friday, May 31, 8:00 a.m. - 11:40 a.m.

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<th>Session 26: High Speed Interconnects &amp; Power Distribution in 3D Integration</th>
<th>Session 27: Wafer Level and Embedded Packaging</th>
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<td>Committee: Electronic Components &amp; RF</td>
<td>Committee: Advanced Packaging</td>
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<tr>
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<td>Mont-Royal 2</td>
<td>Nolita 1</td>
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<tr>
<td>Session Co-Chairs:</td>
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<tr>
<td>Tom Gregorich – Broadcom Corporation</td>
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<tr>
<td>Li Li – Cisco Systems, Inc.</td>
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<tr>
<td>1. 8:00 a.m. – Key Elements for Sub-50µm Pitch Micro Bump Processes</td>
<td>J. DeVos, L. Bogers, T. Buissen, C. Gerets, J. Janierssen, K. Vandersmissen, A. La Manna, and E. Beyne – IMEC</td>
<td>1. 8:00 a.m. – A Study of Wafer Level Package Board Level Reliability</td>
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<tr>
<td>2. 8:25 a.m. – Morphological Characterization of SnAgCu Micro-Bumps for Integration in 3D Interconnects</td>
<td>J. Bertheau, R. Pantel, P. Coutdrian, and N. Hotellerie – STM Microsystems; P. Bleuet and J. Charbonnier – CEA-LETI; E. Hodge – SIMaP-UoMR</td>
<td>2. 8:25 a.m. – Optimization of Solder Height and Shape to Improve the Thermo-Mechanical Reliability of Wafer-Level Chip Scale Packages</td>
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<th>Session 29: Substrates</th>
<th>Session 30: Electrical Modeling and Measurements</th>
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<td>Committee: Materials &amp; Processing</td>
<td>Committee: Modeling &amp; Simulation</td>
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<td>1. 8:00 a.m. – Effect of Strain Rate on Adhesion Strength of Anisotropic Conductive Films (ACF) Joints</td>
<td>1. 8:00 a.m. – Site-Selective Fabrication of Patterned Transparent Copper Mesh on Flexible Substrates at Mild Temperature for Green, Low Cost Electronics</td>
<td>1. 8:00 a.m. – System-Level Clock Jitter Modeling for DDR Systems</td>
</tr>
<tr>
<td>2. 8:25 a.m. – An Approach to Board-Level Drop Reliability Evaluation with Improved Correlation with Use Conditions</td>
<td>2. 8:25 a.m. – The New Primer with Copper Foil Corresponding to Semi-Additive Process for Package Substrates</td>
<td>2. 8:25 a.m. – Circuit/Channel Co-Design Methodology for Multimode Signaling</td>
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<tr>
<td>3. 8:50 a.m. – A New and Effective Drop Test Evolution to Next-Gen Handheld Applications</td>
<td>3. 8:50 a.m. – Dielectric Composite Material with Good Performance and Processibility for Embedding of Active and Passive Components into PCBs</td>
<td>3. 8:50 a.m. – Characterization of a Low-Power, 6.4 Gbps DDR DIMM Memory Interface System</td>
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<tr>
<td>4. 10:00 a.m. – Effect of Aging on High-Strain Rate Mechanical Properties of SAC105 and SAC305 Lead-Free Alloys</td>
<td>4. 10:00 a.m. – An Innovative Embedded Interposer Carrier for High Density Interconnection</td>
<td>4. 10:00 a.m. – Characterization, Modeling, and Optimization of a 3D Embedded Trench Decoupling Capacitors in Si-RF Interposer</td>
</tr>
<tr>
<td>Pradeep Lall, Sandeep Shantaram, and Jeff Suhling – Auburn University; Dave Locker – US AMRDEC</td>
<td>Yu-Hua Chen, Tao-Jiang Tseng, and Dyi-Chung Hu – Unimicron Technology Corporation; Wei-Chung Lo – Industrial Technology Research Institute (ITRI)</td>
<td>Hélène Jacquinot – CEA-LETI; David Denis – IPDIA</td>
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<tr>
<td>5. 10:25 a.m. – Brittle Fracture of Intermetallic Compounds in SAC305 Substrate under High Speed Ball Pull/Pin Pull and Charpy Impact Tests</td>
<td>5. 10:25 a.m. – A Lead-Frame Pre-Mold Coreless Substrate Development</td>
<td>5. 10:15 a.m. – A Novel and Accurate Methodology for Design and Characterization of Wire-Bond Package Performance for 5-10GHz Applications</td>
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<tr>
<td>Chaoran Yang – Hong Kong Univ. of Science &amp; Technology; Guangxi Xu – HKUST LED-FPD; South China Univ. of Technology; S.W. Ricly Lee – Hong Kong Univ. of Science &amp; Technology; HKUST LED-FPD; Xinping Zhang – South China Univ. of Technology</td>
<td>Chang-Yi (Albert) Lan, C.S. Hsiao, Jensen Tsai, Eason Chen, and Otto Hsin – Siliconware Precision Industries Co., Ltd.</td>
<td>Souvik Mukherjee and Django Trombley – Texas Instruments, Inc.</td>
</tr>
<tr>
<td>6. 11:15 a.m. – Effects of Varying Amplitudes on the Fatigue Life of Lead Free Solder Joints</td>
<td>6. 10:50 a.m. – DBC Substrate for Si- and SiC-Based Power Electronics Modules: Design, Fabrication and Failure Analysis</td>
<td>6. 10:50 a.m. – High Frequency Characterization and Analytical Modeling of Through Glass Via (TGV) for 3D Thin-Film Interposer and MEMS Packaging</td>
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<tr>
<td>7. 11:15 a.m. – Effects of Varying Amplitudes on the Fatigue Life of Lead Free Solder Joints</td>
<td>7. 11:15 a.m. – A Monolithic Aluminum Circuit Board Structure</td>
<td>7. 11:15 a.m. – PCB Pin-Field Considerations for 40 Gb/s SerDes Channels</td>
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Program Sessions: Friday, May 31, 1:30 p.m. - 5:10 p.m.

**Session 31: TSV Innovation and Implementation**

**Committee:** Interconnections

**Mont-Royal 1**

**Session Co-Chairs:**
Gilles Poupon – CEA-LETI
Wei-Chung Lo – iTRI

**1. 1:30 p.m. – Through Si Vias Using Liquid Metal Conductors for Reworkable 3D Electronics**
George A. Hernandez, Daniel Martinez, Charles Ellis, Michael Palmer, and Michael C. Hamilton – Auburn University

**2. 1:55 p.m. – Backside TSV Protrusions Induced by Thermal Shock and Thermal Cycling**
Dingzou Zhang and James Jian-Quang Lu – Reneselaer Polytechnic Institute; Klaus Hummler and Larry Smith – SEMATECH

**3. 2:20 p.m. – Microstructure Investigation of TSV Copper Film**
W.N. Putra – Institute of Microelectronics (A*STAR), Nanyang Technological University; H.Y. Li and A.D. Trigg – Institute of Microelectronics (A*STAR); C.L. Gan – Nanyang Technological University

**4. 3:30 p.m. – Via-Middle Through-Silicon Via with Integrated Airgap to Zero TSV-Induced Stress Impact on Device Performance**
Yann Civale, Stefan Van Huylenbroeck, Augusto Redolfi, Wei Guo, Khayshyar Babaei, Patrick Jaenen, Antonio La Manna, Gerald Beyer, Bart Swinnen, and Eric Beyer – IMEC

**5. 5:55 p.m. – Design and Fabrication of Ultra Low-Loss, High-Performance 3D Chip-Chip Air-Clad Interconnect Pathway**
Erdal Uzunlar, Rajeshri Saha, Vachan Kumar, Azad Naemi, and Paul A. Kohl – Georgia Institute of Technology; Rohit Sharma – Indian Institute of Technology Roorkee; Rizwan and Paul A. Kohl – Georgia Institute of Technology; Rohit Sharma – Indian Institute of Technology Roorkee; Rizwan

**6. 4:20 p.m. – Development of Ultra-Low Capacitance Through-Silicon-Vias (TSVs) with Air-Gap Liner**
Qianwen Chen, Cui Huang, and Zheyao Wang – Tsinghua University

**7. 4:45 p.m. – TSV Development, Characterization and Modeling for 2.5D Interposer Applications**
J.R. Tenailleau, P.Voron, and C. Bunel – IPDIA; A. Brunet and S. Borel – CEA-LETI

**Session 32: Thermal and Mechanical Modeling: LED and 3D Structures**

**Committee:** Modeling & Simulation

**Mont-Royal 2**

**Session Co-Chairs:**
Suresh K. Sitaraman – Georgia Institute of Technology; James Jian Zhang – Micron Technology, Inc.

**1. 1:30 p.m. – Drop Impact Simulation and Experimental Validation on High Power Light Emitting Diodes Modules**
Cao Li, Tao Peng, Xuefang Wang, Mingxiang Chen, and Sheng Liu – Huazhong University of Science & Technology

**2. 1:55 p.m. – L70 Life Prediction for Solid State Lighting Using Kalman Filter and Extended Kalman Filter Based Models**
Pradeep Lall and Junchao Wei – Auburn University; Lynn Davis – RTI International

**3. 2:20 p.m. – Effect of Temperature Gradient on Moisture Diffusion in High Power Devices and the Applications in LED Packages**
Xuejun Fan – Lamar University, State Key Lab of Solid-State Lighting; Cadmus Yuan – State Key Lab of Solid-State Lighting, Chinese Academy of Sciences

**4. 3:30 p.m. – Thermal and Mechanical Design and Analysis of 3D IC Interposer with Double-Side Active Chips**
Sheng-Tsai Wu, Heng-Chieh Chien, and John H. Lau – Industrial Technology Research Institute (ITRI); Ting Li, Julia Cline, and Mandy Ji – Rambus, Inc.

**5. 5:55 p.m. – Comparison of Thermal Performance between Glass and Silicon Interposers**
Sangbeom Cha, Yogiendra Joshi, Venkatesh Sundaram, and Rao Trummala – Georgia Institute of Technology; Yoichiro Sato – Asahi Glass

**6. 4:20 p.m. – Simulation of Electromigration through Peridynamics**
Selda Oterkus, John Fox, and Erdogan Madenci – Rice University

**7. 4:45 p.m. – The Effect of Corner Glue on BGA Package Temperature Cycling Performance: A Modeling Study**
Min Pei, Ru Han, Yun Ge, Sanjay Goyal, Vennathry Raparathnam, and Muiffsal Mukadam – Intel Corporation

**Session 33: MEMS and Sensor Packaging**

**Committee:** Advanced Packaging

**Nolita 1**

**Session Co-Chairs:**
S.W. Ricky Lee – Hong Kong Univ. of Science and Technology; James Jian Zhang – Micron Technology, Inc.

**1. 1:30 p.m. – Hermetic Wafer Level Packaging of MEMS Components Using Through Silicon Via and Wafer to Wafer Bonding Technologies**

**2. 1:55 p.m. – Size-Free MEMS-IC High-Efficient Integration by Using Carrier Wafer with Self-Assembled Monolayer (SAM) Fine Pattern**
Jin Lu, Hideki Takeda, and Ryutaro Mameda – National Institute of AIST; Yuka Nakano – National Institute of AIST, Tokyo University of Science

**3. 2:20 p.m. – Outgassing Characterization of MEMS Thin Film Packaging Materials**

**4. 3:30 p.m. – Surface Compliant Bonding Properties of Low-Temperature Wafer Bonding Using Sub-Micron Au Particles**
Hiroaki Ishida and Takuya Yasuki – Sasa MicroTec KK; Toshinori Ogashawa, Yuke Kanehira, and Hiroshi Murai – Tanaka Kikinzoku Kogyo KK; Shin Ito and Jun Mizuno – Waseda University

**5. 5:55 p.m. – Hermetic Wafer-Level Glass Sealing Enabling Reliable Low Cost Sensor Packaging**
Ulli Hansen and Simon Maus – MSG Lithoagas GmbH; Michael Topper – Fraunhofer IZM

**6. 4:20 p.m. – Cu/Sn SLID Wafer-Level Bonding Optimization**
The Thuy Luu, Ani Duan, Kaiying Wang, Knut Asmuthveit, and Nils Hoivik – Vestfold University College

**7. 4:45 p.m. – Reliability of Flip-Chip Technologies for SiC-MEMS Operating at 500°C**
Roderich Zeiser, Lukas Lehmann, Volker Fiedler, and Jürgen Wilde – University of Freiburg

**Refreshment Break: 2:45 p.m. - 3:30 p.m. (Mont-Royal Commons)**
Program Sessions: Friday, May 31, 1:30 p.m. - 5:10 p.m.

### Session 34: New Developments in Wirebond Technology

**Committees:** Assembly & Manufacturing Technology / Interconnections

**Nolita 2**

1. **1:30 p.m.** – Investigation of Charge Induced Bond Pad Corrosion

2. **1:55 p.m.** – Effects of Bond Pad Probing for Cu Wire Bond Packages
   - John D. Beleran, Gaurav Mehta, Ninoy Málanes II, and Nathapon Sathivongsunhorn – United Test and Assembly Center, Ltd. (UTAC); Eu Jin Lee – GLOBALFOUNDRIES

3. **2:20 p.m.** – A Study of Free Air Ball Formation in Palladium-Coated Copper and Bare Copper Bonding Wire
   - Noritoshi Araki, Ryo Oishi, and Takashi Yamada – Nippon Micometal Corporation; Yutsumoto Ichiyama – Nippon Steel Technoresearch Corporation

4. **2:45 p.m.** – Second-Harmonic Nonlinearities in Cu-Wire-Bonded Integrated Circuits

### Session 35: Solder and Bonding

**Committee:** Materials & Processing

**Nolita 3**

1. **1:30 p.m.** – NiFe-Based Ball-Limiting-Metallurgy (BLM) for Microbumps at 50um Pitch in 3D Chip Stacks
   - Bing Dang, Steven Wright, Joana Maria, Cornelia Tsang, Paul Andry, Lowell Wiggins, and John Knickerbocker – IBM Corporation

2. **1:55 p.m.** – The Growth and Segregation of Intermetallic Compounds in the Bulk of Flip Chip Sn2.4Ag Solder Joint under Electrical Current Stressing
   - Wei-Chieh Wang and Kwang-Lung Lin – National Cheng Kung University; Ying-Ts Chiu and Yi-Shao Lai – Advanced Semiconductor Engineering, Inc.

3. **2:20 p.m.** – Voiding Mechanism and Control in BGA Joints with Mixed Solder Alloy System
   - Yan Liu, Derrick Herron, Joanna Keck, and Ning-Cheng Lee – Indium Corporation

4. **2:45 p.m.** – Advanced Materials for Drop in Solution to Pb in High Temp Solder: The Next Generation of Zinc-Based Solder Alloy
   - Jaronng Li and Brian Knight – Honeywell Electronic Materials; Bih-Wen Fon and Shutesh Krishnan – On Semiconductor

### Session 36: System Components for RF and Millimeter Wave

**Committee:** Electronic Components & RF

**Yaletown 4**

1. **1:30 p.m.** – Low Cost BT Organic Material for Wireless 60 GHz Application
   - Poyua Talebeydokht and Mohamed A. Megahed – Intel Corporation

2. **1:55 p.m.** – Novel Enhancement Techniques for Ultra-High-Performance Conformal Wireless Sensors and “Smart Skins” Utilizing Inkjet-Printed Graphene
   - Taoran Le, Ziyin Lin, C.P. Wong, and M.M. Tezzeri – Georgia Institute of Technology

3. **2:20 p.m.** – High Performance Plastic Molded QFN Package with Ribbon Bonding and a Defective PCB Ground
   - Yi-Chieh Lin, Wen-Hsan Lee, Tzyy-Sheng Horng, and Lih-Tyng Hwang – National Sun Yat-Sen University

### Refreshment Break: 2:45 p.m. - 3:30 p.m. (Mont-Royal Commons)

4. **3:30 p.m.** – Single Chip Plated Ni/Pd over ALCAP Bond Pads for Flip Chip Applications and Prototyping
   - Brian J. Lewis, Daniel F. Baldwin, Paul N. Houston, Fei Xie, and Le Hang La – Engert, Inc.

5. **3:55 p.m.** – Low Cost Silver Alloy Wire Bonding with Excellent Reliability Performance

6. **4:20 p.m.** – Corrosion of the Cu/Al Interface in Cu-Wire-Bonded Integrated Circuits
   - John Olsenbach, B.Q. Wang, Sue Erensik, John DeLuca, and Dongmei Meng – LSI Corporation

7. **4:45 p.m.** – Second-Harmonic Nonlinearities in RF Silicon Integrated Passive Devices
1. Adoptable and Integrated Packaging Platform for MEMS-Based Combs Sensors Utilizing Innovative Wafer-Level Packaging Technologies

2. Nonlinear Viscoelastic Constitutive Model for Organic Polymer Composite Materials

3. Bath Chemistry and Copper Overburden as Influencing Factors of the TSV Annealing


5. Glass Carrier Wafers for the Silicon Thinning Process for Stack IC Applications

6. Fast Signal Integrity Methodology for PCB Pre-Layout Electromagnetic Modeling of 3D Integration and Packaging

7. Microwave Induced Plasma Decapsulation of Stressed and Damaged High Count Copper Wire Bonded IC Packages

8. 2D Printed Flexible Functional Materials for High Performance and Fine Pitch Applications

9. Microwave Induced Plasma Decapsulation of Stressed and Damaged High Count Copper Wire Bonded IC Packages

10. Glass Carrier Wafers for the Silicon Thinning Process for Stack IC Applications

11. Reflection-Phase Variation of Cavity-Resonator-Integrated Exciting Surface Laser Mirror for Optoelectronics, Shanghai Jiao Tong University


13. Development of Double Sided with Double-Chip Stacking Based on Cu-Sn Micro-Bump Bonding and TSV for High-Speed, Board-Level Optical Interconnects

14. Impact of Wafer Thinning on High-k Metal Gate 20nm Node Performance

15. Fabrication and Characterization of Novel Polyimide-Based Through-Silicon Via for Silicon Interconnects

16. Electronic-Microfluidic System for Sorting Particles and Applications in Lab-on-Chip Devices

17. Advanced LED Package with Temperature Sensors and Microfluidic Cooling

18. Strength of Solid-State Silver Bonding between Copper and Polysilicon: Experiment and Finite Element Simulation

19. Strength of Solid-State Silver Bonding between Copper and Polysilicon: Experiment and Finite Element Simulation

20. A New 2.5D TSV Package Assembly Approach through Special Patterned Via Forming for High-Density 3D SIP Based on LTCC Packaging Platform

21. A New 2.5D TSV Package Assembly Approach through Special Patterned Via Forming for High-Density 3D SIP Based on LTCC Packaging Platform

22. High Frequency DC-DC Converter with Co-Packaged Planar Inductor and Power IC

23. Strength of Solid-State Silver Bonding between Copper and Polysilicon: Experiment and Finite Element Simulation

24. Strength of Solid-State Silver Bonding between Copper and Polysilicon: Experiment and Finite Element Simulation

25. A Novel 2.5D TSV Package Assembly Approach through Special Patterned Via Forming for High-Density 3D SIP Based on LTCC Packaging Platform

26. A New 2.5D TSV Package Assembly Approach through Special Patterned Via Forming for High-Density 3D SIP Based on LTCC Packaging Platform

27. Novel Design and Reliability Assessment of a 3D DRAM Stacking Based on Co-silicon Micro-Bump and TSV Interconnection Technology

28. Fast Signal Integrity Methodology for PCB Pre-Layout Electromagnetic Modeling of 3D Integration and Packaging with Vertical Interconnects

29. Fast Signal Integrity Methodology for PCB Pre-Layout Electromagnetic Modeling of 3D Integration and Packaging with Vertical Interconnects

30. A New 2.5D TSV Package Assembly Approach through Special Patterned Via Forming for High-Density 3D SIP Based on LTCC Packaging Platform

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Wednesday, May 29, 2013 • 9:00 a.m. - Noon & 1:30 p.m. - 6:30 p.m.  
Thursday, May 30, 2013 • 9:00 a.m. - Noon & 1:30 p.m. - 4:00 p.m.

**Interactive Presentation Sessions**  
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Wednesday, May 29, 2013 afternoon Interactive Presentations • 2:00 p.m. - 4:00 p.m.  
Thursday, May 30, 2013 morning Interactive Presentations • 9:00 a.m. - 11:00 a.m.  
Thursday, May 30, 2013 afternoon Interactive Presentations • 2:00 p.m. - 4:00 p.m.  
Friday, May 31, 2013 Student Interactive Presentations • 8:30 a.m. - 10:30 a.m.

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We are a leading service provider of failure diagnostics and material assessment for industry including semiconductor technologies, microelectronic components, microsystems and nanostructures. We consider the entire work flow from non-destructive defect localization over high precision target preparation to cutting edge nanoanalytics supplemented by micro-mechanical testing, finite element modeling and numerical simulation. We support cooperation partners in introducing innovative materials and technologies, improving manufacturing process steps, securing reliable field use of components, analyzing field returns, and consequently optimizing manufacturing yield, product quality, reliability, and cost efficiency. Due to our close collaboration with leading microelectronics manufacturers, we are able to support test- and diagnostics equipment suppliers in exploring and evaluating upcoming markets and future application fields. Industry partners are provided with innovative hard- and software components, problem-adapted analysis work flows and industry-compatible application str.

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Invisible – but indispensable – nowadays nothing works without highly integrated microelectronics and microsystem technology. Reliable and cost-effective assembly and interconnection technologies are the foundation of integrating these in products. Fraunhofer IZM, a worldwide leader in the development and reliability analysis of electronic packaging technologies, provides its customers with tailor-made system integration technologies on wafer, chip and board level. Our research also ensures that electronic systems are designed to meet the needs of its global customer base. The IZM solutions enable its customers to migrate to newer, more complex designs, while reducing manufacturing time and total cost. Multipayer PCB - Advanced technology high-end printed circuit boards (PCBs) design and manufacturing, as well as high-end servers, FCBGA - Ultra-Thin & High-density wiring structure, applying core layer free, full build-up, and full stacked-via technology.

Fujitsu Interconnect Technologies Limited (FICT), a wholly owned company of Fujitsu Limited of Japan, provides innovative design and manufacturing solutions for package substrates and printed circuit boards (PCBs) to meet the needs of its global customer base. FICT’s solutions enable its customers to migrate to newer, more complex designs, while reducing manufacturing time and total cost. Multipayer PCB - Advanced technology high-end printed circuit boards (PCBs) design and manufacturing, as well as high-end servers, FCBGA - Ultra-Thin & High-density wiring structure, applying core layer free, full build-up, and full stacked-via technology.

High Microsystems™, LLC 250 Cheesquake Road Parlin, NJ 08859 Phone: 800-346-3656 or 512-301-5207 www.hdmicrosystems.com Contact: Kevin DeMartini Kevin.T.Demartini@dundump.com Booths 312 & 314

HD Microsystems is a joint venture company of Hitachi Chemical and DuPont Electronics specializing in spin-applied polyimide (PI) and polybenzoxazole (PBO) wafer dielectric coatings. HDM will highlight new polymeric materials as well as innovative process technologies for WLP and 3D/TSV applications, including stress buffer materials (SB), redistribution dielectric layers (RDL), wafer bonding adhesives (temporary and permanent) and interlayer dielectrics (ILD).

Henkel Electronic Materials 14000 Jamboree Rd. Irvine, CA 92626 Phone: 714-368-8000 Fax: 714-368-2265 www.henkel.com/electronics Contact: Douglass Dixon electronics@us.henkel.com Booth CCS

Henkel offers a complete range of semiconductor packaging materials designed to meet the requirements of today's challenging devices. Our superior technology known through the leading brands of Abastik®, Hysol®, and Multicore® includes die attach pastes, die-attach film dies for stacked package applications, Wafer Backside Coating™ die attach solder, liquid encapsulants, package-level underfills, mold compounds, tacky fluxes and solder spheres.

Heraeus Materials Technology GmbH & Co. KG Heraeusstr 12-14 Hanau 63450 Germany Phone: +49-6181-359617 Fax: +49-6181-35169617 www.heraeus-materials.com Contact: Miriam Elsner miriam.elsner@heraeus.com Booth 308

Worldwide Suppliers of Materials for the Electronics and Semiconductor Market – Heraeus supplies solder paste, sinter paste, fluxes, soft solder wire, solder spheres, solder powders, thermally and electrically conductive adhesives and variety of other adhesives to the package and component assembly markets. Moreover, the Business Unit Bonding Wires provides bonding wires made of gold, aluminum, aluminum alloys and copper, as well as precious and non-precious metal ribbons. The Contact Materials Division of Heraeus offers a wide range of innovative products to address your contact material requirements.

Hesse Mechatronics, Inc. 225 Hammond Avenue Fremont, CA 94539 Phone: (408) 436-9300 Fax: (408) 231-3232 www.hesse-mechatronics.com Contact: Joseph S. Bubel info@hesse-mechatronics.us Booth 110

Hesse Mechatronics, a worldwide company based in Paderborn, Germany, designs and manufactures high speed fine pitch wedge bonders for production of RF, microwave, optoelectronic, military and consumer electronics devices and heavy wire bonders for production of power electronics and automotive devices. The company’s fully automatic wedge bonders handle light and heavy wire applications with aluminum and gold round wire from 12.5 micron (0005) to 500 microns (.020) in diameter, in addition to ribbon wire from 6 x 35 microns up to 3 x 2 mm, including HCR™ (High Current Ribbon). The company’s heavy wire bonders also handle copper wire and ribbon. The NEW Bondjet BJ931 High Speed Fully Automatic Dual-Head Wedge Bonder meets the latest technology and flexibility demands for automotive and power electronics applications.

High Connection Density, Inc. (HCD) 820A Kifer Road Sunnyvale, CA 94086 Phone: 408-743-9700 Fax: 408-743-9701 www.hcdcorp.com Contact: Charlie Stevenson sales@hcdcorp.com Booth 414

High Connection Density, Inc. (HCD) is a premier supplier of board-to-board, flex-to-board, and package-to-board solderless connectors for BGA, LGA and socket applications. HCD’s SuperButton® and SuperSpring® technology-based products are the perfect solution for projects requiring high frequency, high current and low resistance. Designed for manufacturability, HCD offers its innovative proprietary technology at competitive prices.

Huntsman Advanced Materials 10003 Woodloch Forest Dr The Woodlands, TX 77380 Phone: 888-564-9318 Fax: 281-719-4032 www.huntsman.com/advanced_materials Contact: Doug Ellerbusch doug_ellerbusch@huntsman.com Booth 208

Huntsman Advanced Materials is a leading global supplier of synthetic and formulated polymer systems for customers requiring high performance materials which outperform the properties, functionality and durability of traditional materials. In the electronics market, we provide advanced organic protective solutions to build, structure and assemble printed circuit boards and to encapsulate, insulate and bond electrical and electronic components. Our brands, such as Araldite® adhesive and laminating systems, Probum® solder masks and Euremet® hot melt adhesives, are pioneers in the industry, serving customers for more than 50 years. Our customers benefit from sound technical expertise and products that are tailor-made to meet their requirements.

HighTechConnectivity, Inc. (HCD) 250 e. Caribbean Dr. Sunnyvale, CA 94086 Phone: 408-743-9700 Fax: 408-743-9701 www.hcdcorp.com Contact: Charlie Stevenson sales@hcdcorp.com Booth 414

HighTech Connectivity, Inc. (HCD) is a premier supplier of board-to-board, flex-to-board, and package-to-board solderless connectors for BGA, LGA and socket applications. HCD’s SuperButton® and SuperSpring® technology-based products are the perfect solution for projects requiring high frequency, high current and low resistance. Designed for manufacturability, HCD offers its innovative proprietary technology at competitive prices.

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As the world leader in nanomechanical metrology, Hystron® is dedicated to the development of next-generation testing solutions for microelectronics characterization. Hystron provides innovative solutions to industry’s most challenging material integration problems with our comprehensive nanomechanical testing suite of techniques and modular metrology platforms that keep you at the forefront of materials reliability. Stop by our booth to learn about our exciting new developments in microelectronics characterization and for in-depth discussions with our applications specialists about our latest testing solutions. Hystron is continuously redefining what is possible for materials R&D, failure analysis, and process control.

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bhochib@us.ibm.com
Booth 410
IBM Microelectronics - a world leader in semiconductor and packaging technology has formed a Packaging Joint Development Ecosystem with leading assembly, materials, and equipment providers. This ecosystem leverages IBM's research and development resources with synergistic skills from partner companies to solve shared challenges and drive industry leadership in semiconductor flip chip packaging. IBM's packaging technologies raise the bar on product performance, power efficiency, integration and reliability. Advances in semiconductor device performance and the transition to environmentally friendly interconnects drive complexity in the design and implementation of appropriate packaging solutions. Increased use of multi-core processors that drive larger die size, greater I/O counts and enhanced cooling requirements have made the co-development of silicon and packaging solutions essential to the successful implementation of both. It's time to differentiate your semiconductor packaging technology...Smarter technology for a Smarter Planet.

Hysitron, Inc.
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Booth 508
Hysitron is a global leader in scanning probe metrology for materials research and production, focusing on the development of the next generation of metrology solutions. Based in Minneapolis, MN, Hysitron has grown to become a worldwide leader in the design and manufacture of atomic force microscopes. Hysitron’s core competencies include scanning probe metrology, nanomechanical testing, and tribology. Hysitron’s team is dedicated to providing its customers with the most innovative metrological solutions for the investigation of materials. Hysitron’s metrology solutions have enabled the scientific community to push the boundaries of knowledge.

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Booth 111
Industrial Technology Research Institute (ITRI) celebrates 40 year anniversary in 2013, is a non-profit organization conducting in applied research and technological services. Electronics and Optoelectronics Research Laboratories (EOL) is one of the core labs, devoted to advanced researches in semiconductor technologies and optoelectronics developments. EOL has played a key role in Taiwan’s prominent electronic and optoelectronic industries by staying tuned with global trends of technology. EOL has successfully empowered Taiwan and Worldwide partners/industries in further enhancing their competitiveness in manufacturing technologies and product developments.

The core competences of EOL are briefly introduced below:
- NVM Technology
- Roll-to-Roll flexible technology & OLED lighting
- Bio-photonic system and 3D Imaging Technology
- LED Optoelectronic Semiconductor Technology
- 3D IC/3D Integration & SIP Packaging Technology on Si/Glass/AlN;
- Power packing and Intelligent power Module

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joe@zntechologies.com
Booth 408
TDM (Topography and Deformation Measurement) is a patented INSIDIX technology that helps the development engineer increase the reliability of his products, from simple components to highly complex packaging, and allows the failure analysis engineer to understand more accurately the root causes of failures observed in operations. The TDM operating system combines a powerful, internally developed heating/cooling sequence with a sophisticated optical set-up for 3D topography analysis/warpage measurement under thermal stress of all kinds of materials, components and sub-systems. TDM can impose the same thermal profiles and cycles on the devices that they will actually experience during the production process and during normal use. Throughout the thermal cycle, TDM measures the 3D deformation and warpage related to the imposed thermal stress, thus revealing faults that would likely occur during normal production and use.

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info@isipkg.com
Booth 201
Interconnect Systems, Inc. (ISI) is a leading provider of advanced packaging and interconnect solutions for top-tier OEMs in a wide range of industries including military/aerospace, computing/telecom, medical, industrial, and automotive. ISI pioneered the concept of Next Level Integration, an alternative design path that integrates at the module level rather than the silicon level, resulting in lower production costs and faster time-to-market. ISI's breadth of products includes miniaturized FPGA systems, high density modules, 3D and advanced packaging, IC obsolescence adapters, and standard/custom interconnect solutions.

The company's in-depth design and process development knowledge and extensive manufacturing capabilities allow it to quickly execute on Next Level Integration projects and thus provide a comprehensive turnkey solution for its customers.

Invensas
2702 Orchard Parkway
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Booth 114
A global leader in semiconductor interconnect solutions, Invensas invents, productizes and acquires novel technology to provide broader and more complete solutions for its customers. The company uses interconnectology to extend its design capabilities from chip-level to board module and system-level, innovating in areas such as mobile computing and communications, memory and data storage, and 3D-IC technologies.

J-DEVICES Corporation
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Booth 403
J-DEVICES Corporation is a leading OSAT (Outsourced Semiconductor Assembly and Test) company, providing turnkey semiconductor backend services and expanding service capability with an extremely high growth rate. The company's unique mix of advanced packaging and testing technology continues to achieve globally competitive cost and contribute to its customers' success. Besides various types of general packaging such as SOP, QFN, QFP, BGA, FBGA, FCBGA, SIP, PoP, MEMS and CIS packages with best-in-class quality, WFOP (Wafer level Fan Out Package) is one of our innovative milestones aligning to the migration of 3D packaging in the future. We provide 2D/2.5D/3D packaging solutions of outstanding performance with competitive cost. Let your imagination run with what and how WFOP will carry into your products.
Manufacturers for advanced technology nodes.

with high throughput. Mass as an SPC response

Mass metrology provides a rapid inline measurement

control (SPC) of the complete manufacturing sequence.

unprecedented atomic layer accuracy.

change in these ultra-thin steps to be determined with

Patented technology from Metryx enables any mass

a sequence of steps, adding or removing materials.

mark.berry@metryx.net

Contact: Mark Berry

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Phone: +773-418-9916

Nailsea Wall lane, Nailsea

Metryx ltd.

performance.

and is flexible in routing design for enhanced electrical

ceramic technology and multilayer organic technology

core material CPCORE has features of both multilayer

substrates have high density build-up and CPCORE as a

KST created SHDBU substrates for high-speed

circuit boards for high performance, high reliability and

superior substrates for IC packages and high density

technology with thin multilayer structure. We offer

offer superior substrates for IC packages and high density

circuit boards for high performance, high reliability and
good cost performance.

KST created SHDBU substrates for high-speed

applications with high I/O count flip chip BGA. SHDBU

substrates have high density build-up and CPCORE as a core material CPCORE has features of both multilayer ceramic technology and multilayer organic technology and is flexible in routing design for enhanced electrical performance.

KYO CERA SLC Technologies also provides FC-WSPs

in response to the demand for thin and small substrates

for markets such as digital handset equipment.

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Phone: +773-418-9916

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Contact: Mark Berry

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Booth CC10

Metryx manufactures innovative mass metrology

equipment for use in semiconductor manufacturing.

All microelectronic devices are manufactured through a sequence of steps, adding or removing materials. Patented technology from Metryx enables any mass change in these ultra-thin steps to be determined with unprecedented atomic layer accuracy.

The mass response is used to characterize materials and processes, or is implemented in statistical process control (SPC) of the complete manufacturing sequence. Mass metrology provides a rapid inline measurement on product wafers enabling an increase in test coverage with high throughput. Mass metrology has been adopted by 200mm and 300mm Volume Manufacturers for advanced technology nodes.

Moldex3D North America

Moldex3D North America Sales & Support Center

21800 Haggerty Road, Suite 109

Northville, MI, 48167

Phone: 248-946-4570

Fax: 248-928-2270

www.moldex3d.com

Contact: Kenny Lu

kennylu@moldex3d.com

Booth 211

Moldex3D has been providing the professional CAE analysis solution for the plastic injection molding industry since 1995. Moldex3D IC Packaging provides a complete series of molding solutions that help engineers to simulate the complex chip encapsulation process, validate mold design, and optimize process conditions. It helps designers to fully analyze the chip encapsulation process from filling, curing, cooling, to advanced manufacturing demands, such as underfill encapsulation, post-molding annealing, stress distribution, or structural evaluation. Significant molding problems can be predicted and solved upfront, which helps engineers enhance chip quality and prevent potential defects more efficiently. Moldex3D is committed to provide the advanced technologies and solutions for industrial demands, and Moldex3D has extended its worldwide sales and service network to provide local, immediate and professional service.
**NANiUM S.A.**

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Portugal

Phone: +351 252 24 6001
Fax: +351 252 24 6001
www.nanium.com

Contact: Antonio Barny
antonio.barny@nanium.com

Booth 105

NANiUM is a world-class provider of semiconductor assembly, packaging and test engineering and manufacturing services, and a leader in 200mm wafer-level packaging (WLP). The company offers in-house capabilities for the entire development chain, from design to multiple packaging technologies, and the flexibility to tailor solutions that respond to the most specific and demanding customer requirements. Since production start in 2010, more than a quarter billion eWLB components have been shipped. NANiUM is continuously developing new solutions, like System-in-Package (SiP) at the wafer level, to stay at the leading edge of this technology. Since end of 2012, WLCSP based on fan-in technologies is complementing the existing fan-out WLP offer, which targets high pin count and high performance products; SiPs and 3D integration.

Newport Corp.

101 Billerica Ave.
N. Billerica, MA 01862
Phone: 978-667-9449
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dan.crowley@newport.com

Booth 104

Newport is a leading supplier of high precision dispense and assembly equipment for the semiconductor and microelectronics industry offering systems for the manufacture of Microwave, Optical, MCM’s and MEM’s devices. With over two decades of advanced packaging application experience, Newport products support multiple interconnect technologies, including epoxy die bonding, eutectic attach and flip chip. The ultra-precision Newport MRSI-M3 with 3 micron accuracy, MRSI-MS with 5 micron accuracy and MRSI-605 Assembly Work Cells specialize in thin die handling and 3D packaging and the Newport MRSI-175Ag Epoxy Dispenser is the leader for high precision conductive epoxy dispensing including 125 micron dots.

Nikon Metrology, Inc.

12701 Grand River Avenue
Brighton, MI 48116
Phone: 810-220-4300
Fax: 810-220-4300
www.nikonmetrology.com

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marketing_us@nikonmetrology.com

Booth 98

Nikon Metrology offers the most complete metrology product portfolio, including X-Ray and Computed Tomography inspection systems and state-of-the-art vision measuring instruments featuring optical and mechanical 3D metrology solutions. These innovative metrology solutions respond to the advanced inspection requirements of manufacturers active in aerospace, electronics, automotive, medical, consumer and other industries.

Nordson DAGE

48065 Fremont Boulevard
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Fax: 510-933-2966
www.nordsondage.com

Contact: Aram Kardjian
aram.kardjian@nordsondage.com

Booth 416

Nordson DAGE is the market leading provider of award winning test and inspection systems for mechanical testing of electronic components and is recognized as an industry standard. The 4000PLUS platform compliments the 4000 series test systems, for advanced bondtesting such as wire, lead and ribbon pull, BGA sphere and package fatigue, PCB 3 point bend testing, hot bump pull for PCB pad cratering testing in accordance with IPC9708, and shear testing. The 4000HS high speed bondtester, capable of testing solder bumps in high speed shear and high speed cold bump pull modes, is becoming a viable alternative to board level drop testing. The 4000HS, in addition to total and fractional values, provides bond energy results, proving invaluable for failure mode analysis the detection of lead-free brittle fractures.

NTK Technologies, Inc.

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scdinfo@ntktech.com

Booth 116

NTK is a global leader in Organic and Ceramic Packaging. NTK’s Packaging is aligned to support custom designs with varying volume requirements. Our package design support is geared to stream-line electrical and thermal design optimization. Materials include HTCC, LTCC, and a variety of Organic and Lamine Materials and Technologies. NTK’s proven simulation tools have enabled optimum package design for high speed communications in the 10G, 40G, 100G, and soon approaching 400G for both, ceramic and organic packages. Advanced ceramic-based applications available for Space Transformers for Probe, CCD and CMOS Image Sensors.

Ormet Circuits / NSCC

6555 Nancy Ridge Drive #200
San Diego, CA 92121
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Fax: 858-455-7108
www.ormetcircuits.com

Contact: Peter Matturri
Support@ormetcircuits.net

Booth 516

Ormet and NSCC welcome you to visit exhibit 516 introducing new products for semiconductors interconnect markets. Ormet Circuits, Incorporated (Ormet) is a privately held company, engaged in the design, manufacture, and sale of conductive pastes for use in the manufacture of advanced electronic devices. Ormet pastes are lead-free, highly electrically and thermally conductive and provide good intermetallic joints at relatively low temperatures.

Nippon Steel & Sumikin Chemical Co., Ltd., as a core member of the Nippon Steel & Sumitomo Metal Corp. Group, is the key industr

PAC TECH USA – Packaging Technologies, Inc.

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Booth 301

Packaging Technologies GmbH (PAC TECH), a group member of NAGASE & CO., Ltd., is comprised of two unique business units: Advanced Packaging Equipment Manufacturing; Automatic wet chemical lines for high volume electroless NiAu & NiPdAu bumping (PacLine 300 ASU), laser soldering equipment (SB2 Jet), wafer-level solder ball transfer systems (Ultra-SB2), and laser-assisted flip-chip bonders (Laplace).

Wafer Level Packaging & Bumping Services: Subcontract wafer bumping with electroless Ni/Au or Ni/Pd under-bump metallization (UBM) for FC or WLCSP solder bumping, as well as NiPdAu for wire bonding. PAC TECH also offers AOI, X-Ray, RDL, Thinning, Backmetall, Laser Marking, Dicing and Tape & Reel.

Headquartered in Nauen, Germany, PAC TECH has 100% subsidiaries: PAC TECH US - Packaging Technologies Inc. (Silicon Valley, USA) & PAC TECH ASIA Sdn. Bhd. (Penang, Malaysia).

Palomar Technologies

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Booth CC6

Palomar Technologies, a former subsidiary of Hughes Aircraft, is the global leader of automated high-accuracy, large work area die attach and wire bond equipment and precision contract assembly services. Customers utilize the products, services and solutions from Palomar Technologies to meet their needs for optoelectronic packaging, complex hybrid assembly and micron-level component attachment.

Palomar Technologies Assembly ServicesTM ("Assembly Services"), located in Carlsbad, CA, is the contract assembly, process development, test and prototyping division of Palomar Technologies. Assembly Services provides process expertise with high-precision die attach, wire bond and component placement services, offering its customers an alternative route to meet complex packaging needs for without investing in capital equipment.

PURE TECHNOLOGIES

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www.puretechnologies.com

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Booth 307

Pure Technologies manufactures low (<0.001 cph/cm²), ultra-low (>0.001 cph/cm²) alpha emitting Sn (Sn). Lead-Free (including all SAC) alloys, Pb and Pb/Sn alloys. These ALPHA®OLO® products are available in various shapes and sizes - ingots, anodes, slugs, pellets, foil, rods, biscuits, PBC and SnO powder, etc. for wafer-level packaging, interconnects, and sphere and powder/paste manufacturing. ALPHA-LO® reduces or eliminates soft errors from alpha particle emissions from soldiers, enhances performance reliability and reduces corporate liability. All materials are guaranteed and certified to be at secular equilibrium and are tested and retested over time before shipping to insure that the alpha emission rate is stable and will not increase over time.
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Fax: 707-255-9079
www.royceinstruments.com
Contact: Casey Krawiec
casey@royceinstruments.com

Book 311
Royce Instruments is your preeminent supplier of Bond Testing and Die Sorting equipment. The new 600 Series of Bond Test Instruments brings unparalleled networking capability and scalability to the bond test market. With a choice of 3 bond testers, Royce offers an instrument solution to meet the evolving needs of manufacturers and institutions worldwide. Royce Die Sorters (AutoPlacer MP300 and DE3S-ST) offer fully-automatic and semi-automatic die sorting solutions for today’s challenging applications, including die as small as 200 um square or 50 um thick. For sensitive products where the device surface cannot be touched (i.e., MEMS), non-surface contact is available that grips the device from the edges. With quick tooling change-outs, wafer mapping, and die inverter and inspection options, Royce Die Sorters are ideal for high mix, medium volume applications.

RTI International - Center for Materials & Electronic Technologies
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P.O. Box 12194
RTP, NC 27709
Phone: 919-248-1801
www.rti.org/microsystem
Contact: Alan Huffman
huffman@rti.org

Book 310
RTI International’s Center for Materials and Electronic Technologies is a world leader in advanced interconnect and packaging technologies conducting R&D in sensors and actuators, electronic material characterization, and novel microfabrication. RTI provides state of the art wafer bumping and WLP technologies, supporting small- and mid-volume customers as well as developmental applications. A recognized leader in 3D integration, RTI works with commercial, government, and academic clients to develop and implement solutions. Fully integrated fabrication and analytical facilities allow RTI to support a diverse project base, from process development, proof of concept and prototyping, to small-scale production. The Center is staffed with seasoned engineers and researchers developing new technologies and solutions. RTI is a non-profit research institute offering innovative research, technical expertise, and fabrication capabilities to governments and businesses worldwide.

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Book CCB
Rudolph Technologies is a leader in the design, development, manufacture and support of defect inspection, advanced packaging lithography, process control metrology, and data analysis systems and software used by semiconductor device manufacturers worldwide. Rudolph’s product suite offers hardware and software solutions for the demanding requirements of the advanced packaging market, including 2D/3D bump inspection, RDL and overlay metrology, and a lithography stepper specifically designed for the back-end. Turn data into useful information with Rudolph’s powerful solutions including run-to-run control, fault detection and classification and yield management systems.

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glecarpentier@set-sas.fr

Book 311
SET – Smart Equipment Technology (Former Suss MicroTec Device Bonder Division) is a world leading supplier of High Accuracy Assembly and Nano Imprint Lithography Solutions. As a supplier of semiconductor equipment dedicated to high-end applications for over 30 years and with more than 300 Device Bonders installed worldwide, SET is globally renowned for the unsurpassed bonding accuracy (± 0.5 µm) and the high flexibility of its die and flip-chip bonders. SET’s product portfolio ranges from manual loading versions to fully automated operation. The SET systems cover a wide range of bonding applications and offer the unique ability to handle both fragile and small components onto substrates up to 300mm.

Shin-Etsu MicroSi, Inc.
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Shin-Etsu MicroSi, Inc. is a wholly owned subsidiary of Shin-Etsu Chemical Ltd. Shin-Etsu MicroSi is a world class supplier of packaging materials for the semiconductor industry. With a global support network, which includes Sales Engineers, R&D, Manufacturing, Quality Assurance, and Logistics, we are able to quickly develop and provide new technologies to benefit our customers. This allows our clients to meet their ever changing technical, commercial and environmental needs by implementing Shin-Etsu MicroSi’s technology. Shin-Etsu MicroSi is known for supplying high performance Thermal Interface Materials, Underfills, Molding Compounds, High Purity Silicone Encapsulants, and Die Attach Materials.

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Shinko Electric Industries Co., LTD. is a leading manufacturer of a wide variety of materials used in the packaging of integrated circuits such as: Organic Substrates, Leadframes, TO-Heaters and Heatspreaders. With headquarters located in Nagano, Japan and offices worldwide, Shinko strives to provide the ultimate in service and solutions for our customers. For more about Shinko please visit our website at www.shinko.com.
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SPTS Technologies designs, manufactures, sells, and supports etch, PVD, CVD and thermal wafer processing solutions for the MEMS, advanced packaging, LEDs, high speed RF on GaAs, and power management device markets. With manufacturing facilities in Newport, Wales, Allentown, Pennsylvania, and San Jose, California, the company operates across 19 countries in Europe, North America and Asia-Pacific. For more information about SPTS Technologies, please visit www.spts.com.

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STATS ChipPAC is a leading service provider of semiconductor design, wafer bump, probe, packaging and test solutions for the communications, digital consumer and computing markets. With advanced process technology and a global manufacturing presence spanning Singapore, South Korea, China, Malaysia and Taiwan, STATS ChipPAC provides innovative and cost effective semiconductor solutions. STATS ChipPAC has a leadership position in advanced package technology such as fan-in and fan-out wafer level packaging, flip chip interconnect, Through Silicon Via (TSV) and 3D integration to meet the increasing market demand for next generation devices with higher levels of performance, increased functionality and compact sizes.

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With more than 60 years of engineering experience, SUSS MicroTec is a leading supplier of process equipment for microstructuring in the semiconductor industry and related markets. Our portfolio covers a comprehensive range of products and solutions for backend lithography, wafer bonding and photomask processing, complemented by micro-optical components.

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Tamar Technology develops and manufactures high-speed non-contact metrology solutions for 3DIC advanced packaging and related processes for MEMS, CMOS image sensors, compound semiconductors, LED, and other market areas. Tamar’s proprietary sensor technology offers maximum flexibility and includes their Optical Stylus Probe (OSP), Wafer Thickness Sensor (WTS), and Visible Thickness Sensor (VTS) to support a variety of applications.

The measurement capabilities include through silicon via (TSV) depth with unlimited aspect ratio, wafer thickness and total thickness variation (TTV) for single and multi-layer wafers, remaining silicon thickness (RST), wafer shape, thin Si thickness, thick films and polymer thickness, and other critical measurement requirements. Tamar’s WaferScan system is modular in design and can be configured for semi or fully automated operation for process development or HVM monitoring.

SUSS MicroTec is now offering materials and equipment to enable 3D IC trade-off cost models are offered. TechSearch International professionals have an extensive network of more than 15,000 contacts in North America, Asia, and Europe and travel extensively, visiting major electronics manufacturing operations and research facilities worldwide.

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Teledyne Microelectronics is a full service microelectronics contract manufacturer offering innovative approaches in high density packaging and testing of micrcocircuits, multichip modules and multichip assemblies. In both our facilities in Los Angeles, California and our future production facility in Lewisburg, Tennessee, we specialize in high density microcircuits utilizing the latest advanced packaging techniques. Areas of high expertise include FBGA, 3D stacking, RF/microwave packaging design and assembly as well as optoelectronics XCVRs, analog/digital circuits.

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For over 50 years, TOK has been supplying superior quality chemicals and equipment to the microelectronics and semiconductor manufacturers of the world. TOK is now offering materials and equipment to enable fabrication of 3DIC with TSVs. These products include photoresists for plating (Au, Ni, Cu, Pb/Sn, SN/Ag), photo definable insulators, and other materials targeted for TSV, RDL, and MEMS applications. Please visit our booth to learn more about TOK’s products and how TOK can help you solve your most challenging advanced packaging requirements.
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Toray Engineering Co., Ltd provides Flip Chip Bonding Equipment for Semiconductor Packaging (FC 2000), Optoelectronics (OF2000) and LCD devices (CL2000FW, OS2000). Also, Vacuum Encapsulation System (VES00) and various Flexible substrates (TCP, interposer) manufacturing equipment such as resist equipment, proximity exposure etching, developing line are available.

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Toray Industries is a leading provider for Non-Conductive Film (NCF) for flip chip packages. Toray’s unique polyimide and film processing technologies provide excellent reliability and performance which are already proven in the market. For over 3 years Toray’s NCF has been used for mass production. For more information on Toray’s products visit www.toray.co.jp/english/electronic

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Torrey Hills Technologies is a California based manufacturer of tungsten-copper, molybdenum-copper, Cu/Mo/Cu and Cu/Mo70Cu/Cu heat sinks commonly used in the electronics industry. These products have high thermal conductivity and provide excellent CTE matches. The company is also distributor of conveyor belt furnaces, including fast firing and infrared furnaces that are widely used in PCB assembly, surface mount technology, semiconductor packaging and solar cell processing industries. Torrey Hills Technologies has been an INC 50005000 for 4 consecutive years.

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Triton Micro Technologies is the leader in the design and manufacture of high-performance 2.5D and 3D Through Glass Via (TGV) interposers. As we rapidly approach the barrier and performance limits of silicon, the need increases for a greater number of components in smaller package areas and the need for non-silicon based materials to better support this next generation assembly.

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The Electronic Components and Technology Conference (ECTC) is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Components, Packaging and Manufacturing Technology (CPMT) Society of the IEEE. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the areas including, but not limited to as given below under each technical subcommittee name. Authors are encouraged to review the sessions of the previous ECTC programs to determine the committee selection for their abstracts.

Advanced Packaging:
3D integration, embedded, and wafer level packaging, flip chip, advanced substrates, novel assembly technologies, interposers, TSVs, MEMS & sensors, electronic (digital, analog, & RF), and optoelectronic & photovoltaic device packaging.

Applied Reliability:
3D package reliability, characterization and test methods, interconnection reliability; solder and material characterization, and next generation/novel packaging reliability.

Assembly and Manufacturing Technology:
Assembly challenges and solutions, manufacturing aspects of 3D/TSV, manufacturing challenges of wafer thinning and flip chip processing.

Electronic Components & RF:
Components (including embedded components) and modules for RF/THz systems and bio applications, metamaterials, wireless sensors, RFID, RF MEMS, flexible & printed electronics, "green" RF electronics, wireless power transmission, power scavenging components, nano-based RF structures, and low-power RF designs.

Emerging Technologies:
Emerging packaging concepts and technologies, emerging 3D packaging concepts, novel approaches to packaging, organic IC & TFT, microfluidics and MEMs, anti-counterfeiting packaging, and packaging for biosensing.

Interconnections:
First- and second-level interconnections: designs, structures, processes, performance, reliability, test including TSV, Si interposer, and interconnections for 3D integration, flip chip, solder bumping and Cu-pillar, wafer-level packaging, advanced wirebonds, non-traditional interconnections (e.g. ECA, CNT, graphene, optical, etc), electromigration for 2.5D and 3D, substrates and PCB solutions for the next generation systems, system packaging and heterogeneous integration.

Materials & Processing:
Adhesives and adhesion, lead free solder, novel materials and processing; underfills, mold compounds, and dielectrics, emerging materials and processing for 3D.

Modeling & Simulation:
Thermal, mechanical, electrical modeling and related measurements, 3D/TSV design and modeling, signal and power integrity, fracture and warpage in packages, material and fabrication modeling, first-level and second-level interconnects, high-speed interconnects.

Optoelectronics:
Fiber optical interconnects, active optical cables, parallel optical transceivers, silicon and III-V photonics devices, optical chip-scale and heterogeneous integration, micro-optical system integration and photonic system-in-package, optoelectronic assembly and reliability, materials and manufacturing technology, high-efficiency LEDs and high power lasers, and integrated optical sensors.

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Papers may be submitted on any of the listed major topics; presentation of papers in an interactive format is highly encouraged at ECTC. Interactive presentations allow significant interaction between the presenter and attendees, and are especially suited for material that benefits from more explanation than is practical for oral presentations. Highly rated abstracts not fitting the theme of an oral session or submitted specifically for interactive presentation, and abstracts that are selected at the discretion of the program chair are included in the Interactive Presentation sessions.

Professional Development Courses
In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses (4 hours) on topics described in the Call for Papers. Using the format “Course Objectives/ Course Outline/Who Should Attend,” 200-word proposals must be submitted via the website at www.ectc.net by October 14, 2013. If you have any questions, contact:

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You are invited to submit a <750-word abstract that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net. If you have any questions, contact:

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Abstracts must be received by October 14, 2013. All abstracts must be submitted electronically at www.ectc.net. You must include the mailing address, business telephone number and email address of presenting author(s) and affiliations of all authors with your submission.
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Lake Buena Vista, Florida, USA • May 27 - 30, 2014

The fun and splendor of Walt Disney World and the greater Orlando area awaits you in 2014. In the heart of the Walt Disney World® Resort, the award-winning Walt Disney World Swan and Dolphin Resort is your gateway to Central Florida’s greatest theme parks and attractions. The resort is located in between Epcot® and Disney’s Hollywood Studios™, and nearby Disney’s Animal Kingdom® Theme Park and Magic Kingdom® Park. Come discover our 17 world-class restaurants and lounges, sophisticated guest rooms with Westin Heavenly Beds® and the luxurious Mandara Spa. Enjoy five pools, two health clubs, tennis, nearby golf, and many special Disney benefits, including complimentary transportation to Walt Disney World Theme Parks and Attractions, and the Extra Magic Hours benefit.

Just minutes from the Walt Disney World Swan and Dolphin Resort is Downtown Disney’s West Side and Marketplace. Downtown Disney’s West Side showcases top-notch restaurants, a 24-screen AMC Pleasure Island movie theater, and other uncommon shops. Here you’ll also find the exquisite Cirque du Soleil La Nouba live entertainment show and the DisneyQuest Indoor Interactive theme park.

Downtown Disney Marketplace provides an appealing place to take a break from Disney Theme Parks and Water Parks. Check out the largest Disney character store in the world. Or, for more of a respite, relax and dine at a lakeside restaurant.

Should you decide to explore outside the Greater Lake Buena Vista area, Orlando boasts other parks and recreation areas tailor made for whatever your pleasure. Favorites include Universal Orlando, SeaWorld, Gatorland, and Winter Park.

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## Conference At A Glance

**Monday, May 27, 2013**
- 3:00 p.m. – 5:00 p.m.
  - PM PD Course Break
  - Mont-Royal Course Break
- Chelsea Commons, 4th Floor
- Registration – Chelsea Commons, 4th Floor

**Tuesday, May 28, 2013**
- 6:45 a.m. – 8:15 a.m.
  - AM PD Courses
  - Registration Only
- Registration – Chelsea Commons, 4th Floor
- 7:00 a.m. – 7:45 a.m.
  - AM PD Courses Instructor and Proctors Briefing & Breakfast
- Chelsea 2
- 7:00 a.m. – 5:00 p.m.
  - Speakers Prep
- Yaletown 3
- 8:00 a.m. – Noon
  - Sessions 1, 2, 3, 4
  - See pages 10 thru 11 for Locations
- 9:00 a.m. – 11:00 a.m.
  - Session 37: Interactive Presentations 1
  - Chelsea 3 & 4
- 9:15 a.m. – 10:00 a.m.
  - Refreshment Break
  - Chelsea 3 & 4
- Noon
  - PD Courses Luncheon
  - Chelsea 2
- 1:00 p.m. – 5:00 p.m.
  - Technology Corner Set-up
  - Chelsea 3 & 4
- 1:15 p.m. – 5:00 p.m.
  - Conference Registration
  - Chelsea Commons, 4th Floor
- 1:15 p.m. – 5:15 p.m.
  - PD PM Courses
  - See page 8 for locations
- 2:00 p.m. – 4:30 p.m.
  - Special Modeling Session
  - Condesa 3, 2nd floor
- 3:00 p.m. – 3:20 p.m.
  - AM PD Course Break
  - Chelsea 2
- 5:00 p.m. – 6:00 p.m.
  - ECTC Student Reception
  - Chelsea 2
- 6:00 p.m. – 7:00 p.m.
  - General Chair’s Speakers Reception (by Invitation)
  - Outside Pool Area, 4th floor, facing the Las Vegas Strip
  - (Rain backup: Chelsea 2)
- 7:30 p.m. – 9:00 p.m.
  - Panel Session
  - Mont-Royal I & 2, 4th floor

**Wednesday, May 29, 2013**
- 6:45 a.m. – 4:00 p.m.
  - Conference Registration
  - Chelsea Commons, 4th Floor
- 7:00 a.m. – 7:45 a.m.
  - Today’s Speaker’s Breakfast
  - Chelsea 1
- 7:00 a.m. – 5:00 p.m.
  - Speakers Prep
  - Yaletown 3
- 8:00 a.m. – 11:40 a.m.
  - Sessions 1, 2, 3, 4
  - See pages 10 thru 11 for Locations
- 9:00 a.m. – 11:00 a.m.
  - Session 38: Interactive Presentations 2
  - Chelsea 3 & 4
- 9:15 a.m. – 10:00 a.m.
  - Refreshment Break
  - Chelsea 3 & 4
- Noon
  - Conference Registration
  - Chelsea Commons, 4th Floor
- 1:30 p.m. – 6:30 p.m.
  - Technology Corner Exhibits
  - Chelsea 3 & 4
- 1:30 p.m. – 5:10 p.m.
  - Sessions 7, 8, 9, 10, 11, 12
  - See pages 12 thru 13 for Locations
- 2:00 p.m. – 4:00 p.m.
  - Session 39: Interactive Presentations 3
  - Chelsea 3 & 4
- 2:45 p.m. – 3:30 p.m.
  - Refreshment Break
  - Chelsea 3 & 4
- 5:30 p.m. – 6:30 p.m.
  - Technology Corner Reception
  - Chelsea 3 & 4
- 7:00 p.m. – 9:00 p.m.
  - Plenary Session
  - Mont-Royal I & 2, 4th floor

**Thursday, May 30, 2013**
- 7:00 a.m. – 5:00 p.m.
  - Speakers Prep
  - Yaletown 3
- 7:00 a.m. – 7:45 a.m.
  - Today’s Speaker’s Breakfast
  - Chelsea 1
- 7:30 a.m. – 4:00 p.m.
  - Conference Registration
  - Chelsea Commons, 4th Floor
- 8:00 a.m. – 11:40 a.m.
  - Sessions 13, 14, 15, 16, 17, 18
  - See pages 14 thru 15 for Locations
- 9:00 a.m. – 11:00 a.m.
  - Session 40: Interactive Presentations 4
  - Chelsea 3 & 4
- 9:15 a.m. – 10:00 a.m.
  - Refreshment Break
  - Chelsea 3 & 4
- Noon
  - ECTC Luncheon
  - Chelsea 1 & 5
- 1:30 p.m. – 6:30 p.m.
  - Technology Corner Exhibits
  - Chelsea 3 & 4
- 1:30 p.m. – 5:10 p.m.
  - Sessions 19, 20, 21, 22, 23, 24
  - See pages 16 thru 17 for Locations
- 2:00 p.m. – 4:00 p.m.
  - Session 41: Interactive Presentations 5
  - Chelsea 3 & 4
- 2:45 p.m. – 3:30 p.m.
  - Refreshment Break
  - Chelsea 3 & 4
- 6:30 p.m. – 7:30 p.m.
  - Gala Reception
  - Chelsea 1 & 5
- 8:00 p.m. – 10:00 p.m.
  - CPMT Seminar
  - Mont-Royal I & 2, 4th floor

**Friday, May 31, 2013**
- 7:00 a.m. – 5:00 p.m.
  - Speakers Prep
  - Yaletown 3
- 7:00 a.m. – 7:45 a.m.
  - Today’s Speaker’s Breakfast
  - Chelsea 1
- 7:30 a.m. – Noon
  - Conference Registration
  - Chelsea Commons, 4th Floor
- 8:00 a.m. – 11:40 a.m.
  - Sessions 25, 26, 27, 28, 29, 30
  - See pages 18 thru 19 for Locations
- 9:00 a.m. – 11:00 a.m.
  - Session 42: Interactive Presentations 6
  - Chelsea 3 & 4
- 9:15 a.m. – 10:00 a.m.
  - Refreshment Break
  - Chelsea 3 & 4
- Noon
  - Program Chair Luncheon
  - Chelsea 1 & 5
- 1:30 p.m. – 5:10 p.m.
  - Sessions 31, 32, 33, 34, 35, 36
  - See pages 20 thru 21 for Locations
- 2:04 p.m. – 3:30 p.m.
  - Refreshment Break
  - Mont-Royal Commons