Advance Program and Registration on-line: www.imaps.org/devicepackaging

IMAPS 9th International Conference and Exhibition on

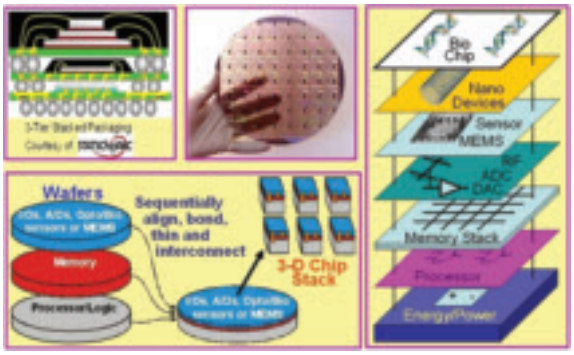
Device Packaging

March 11 - 14, 2013

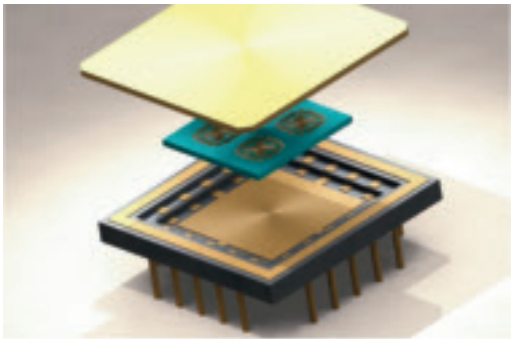
Radisson Fort McDowell Resort and Casino
Scottsdale/Fountain Hills, Arizona - USA

in conjunction with the Global Business Council (GBC) Spring Conference
March 10 - 11, 2013 - www.imaps.org/gbc

IMAPS Global Business Council



Courtesy of Rensselaer Polytechnic Institute



Courtesy of U. S. Army RDEDCOM AMRDEC

General Chair:
James Lu, Rensselaer Polytechnic Institute

General Chair-Elect (PDC):
Ron Huemoeller, Amkor Technology

Past General Chair (Panels):
Peter Elenius, E&G Technology Partners

Technical Chairs:
Rozalia Beica, LAM Research AG
Peter Ramm, Fraunhofer EMFT
Linda Bal, Freescale Semiconductor
Luu Nguyen, Texas Instruments
Tracy Hudson, U. S. Army RDECOM AMRDEC
Russell Shumway, Amkor Technology
Thomas Goodman, E&G Technology Partners
Bob Karlicek, Rensselaer Polytechnic Institute

DPC/GBC Premier Sponsors:

SSEC
Amkor Technology
ASE GROUP

Device Packaging Program Overview

Monday, March 11
10 Professional Development Courses - 1/2 Day
Five - 8:00 am - Noon & Five - 1:00 pm - 5:00 pm

Tuesday, March 12 - Thursday, March 14
Technical Sessions

Tuesday, March 12
Flip Chip/WLP Panel Discussion: 7:00 pm - 8:30 pm

Wednesday, March 13
Poster Session in Exhibit Hall: 2:00 pm - 4:30 pm

3D Panel Discussion: 6:00 pm - 7:30 pm
3D Integration - Applications and Production Challenges

Exhibition

Tuesday, March 12
10:00 am - 7:00 pm

Wednesday, March 13
12:00 pm - 4:30 pm

Organized by: International Microelectronics Assembly and Packaging Society (IMAPS)
Bringing Together the Entire Microelectronics Supply Chain!

Hotel Cut-off: February 8, 2013
Early Registration & Exhibit Deadlines: February 8, 2013

ADVANCED PACKAGING SINGLE WAFER WET PROCESSING

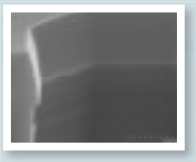
Solid State Equipment LLC

ADVANCED PACKAGING
SINGLE WAFER
WET PROCESSING

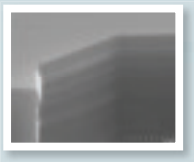
TSV RESIST STRIP AND CLEAN

As received – post DRIE

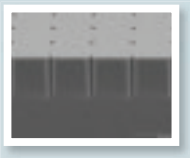
After SSEC Cleaning



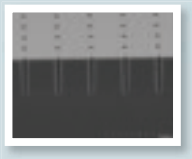
As received – post DRIE



After SSEC Cleaning

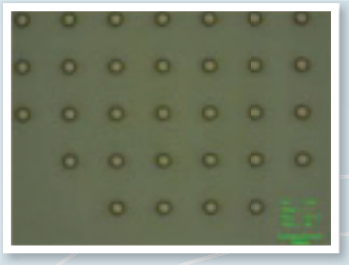


As received – post DRIE

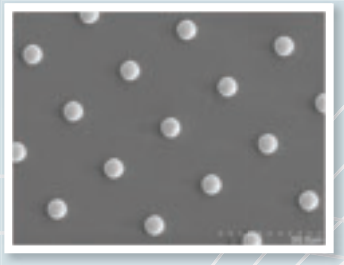


After SSEC Cleaning

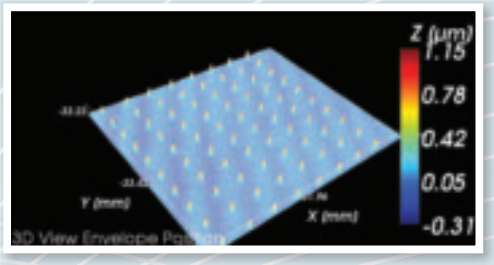
Si ETCH TO REVEAL Cu TSV



Optical

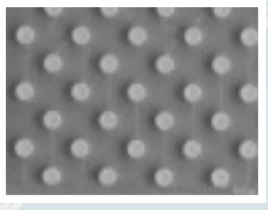


SEM

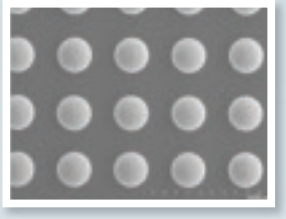


ISIS 3D

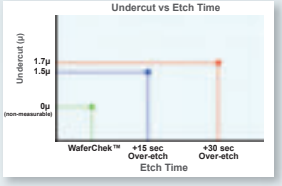
DRY FILM STRIP

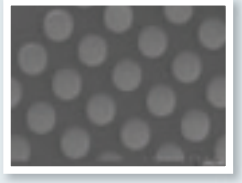


FLUX CLEANING

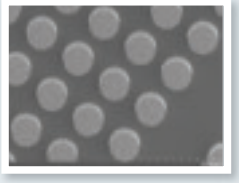


UBM AND RDL METAL ETCH





UBM Post Etch



UBM Post Strip

ssecusa.com

Conference Overview

The 9th annual Device Packaging Conference (DPC2013) will be held in Scottsdale, Arizona, on March 11-14, 2013. It is an international event organized by the International Microelectronics Assembly and Packaging Society (IMAPS).

The conference is a major forum for the exchange of knowledge and provides numerous technical, social and networking opportunities for meeting leading experts in these fields. The conference will attract a diverse group of people within industry and academia. It provides a chance for educational interactions across many different functional groups and experience levels. **People who will benefit from this conference include: scientists, process engineers, product engineers, manufacturing engineers, professors, students, business managers, sales and marketing.**

The 2013 conference will feature technical sessions, panel discussions, a poster session, professional development courses and a vendor exhibition and technology showcase. The conference provides a focused forum on the latest technological developments in 4 topical workshop tracks related to microelectronic packaging: **Advanced 3D Packaging; Flip Chip & Wafer Level Packaging; MEMS & Associated Microsystems; and LED Packaging for Future Solid-State Lighting.**

The professional development courses offered are also focused on these topical areas of microelectronics and offer an additional valuable resource to attendees. The Global Business Council (GBC) will co-locate its Spring Conference March 10-11, focusing on the business aspects of these technologies. There will be several networking receptions and gatherings throughout the week, including the opening reception, meals, and other social events.

Organizing Committee

Advanced 3D Packaging

Technical Chairs:
Rozalia Beica, LAM Research AG

Peter Ramm, Fraunhofer IZM, Munich

Committee:
Franck Murray, IPDIA

Harry Hedler, Siemens Munich

Jeff Calvert, DOW Electronic Materials

Keith Cooper, SET NA

Kuan-Neng Chen, National Chiao Tung University

Muhannad Bakir, Georgia Institute of Technology

Paul Siblerud, Applied Materials

Phil Garrou, Microelectronic Consultants of NC

Reinhard Pufall, Infineon Technologies

Subhash Shinde, Sandia National Laboratories

Thorsten Matthias, EV Group

Yann Guillou, SEMI Europe

Flip Chip & Wafer Level Packaging

Technical Chairs:
Linda Bal, Freescale Semiconductor

Luu Nguyen, Texas Instruments

Committee:
Lars Boettcher, Fraunhofer IZM

Eric Huenger, Dow Chemical

Alan Huffman, RTI International

Jamin Ling, Kulicke & Soffa Industries, Inc.

Gilles Poupon, LETI

Andy Strandjord, PacTech USA

Ted Tessier, Flip Chip International

MEMS

Technical Chairs:
Tracy Hudson, U.S. Army

Russell Shumway, Amkor Technology

Committee:
Thomas Baginski, Auburn University

Robert Dean, Auburn University

Li-Anne Liew, NIST

Phil Reiner, CGI Federal Systems

Peter Tortorici, Medtronics

Alexander Trusov, Univ. CA - Irvine

Keith Warren, MEMS Consultant

High Brightness LEDs

Technical Chairs:
Thomas Goodman, E&G Technology Partners

Bob Karlicek, Rensselaer Polytechnic Institute

Committee:
Sheng Liu, Huazhong Univ of Science & Tech

Ricky Lee, HKUST

Jay Liu, Shineon Technology Co.

GBC Speaker Dinner Sponsors:

SSEC ASE GROUP Amkor Technology KYOCERA

Monday, March 11th

Welcome Reception: 5:00 pm - 6:30 pm

(GBC Attendees Invited)

followed by the...

2013 Texas Hold'em Tournament: 7:00 pm - 10:00 pm

Benefits the IMAPS Microelectronics Foundation

The IMAPS Microelectronic Foundation is holding its third annual charity Texas Hold'em Tournament on March 11th at 7:00 pm. The number of seats at the tables is limited to the first 30 players, and on a first come first served basis, so sign up now online at:
http://www.imaps.org/DevicePackaging/holdem2013.htm for more information.

Amkor presents the building blocks for next generation packaging

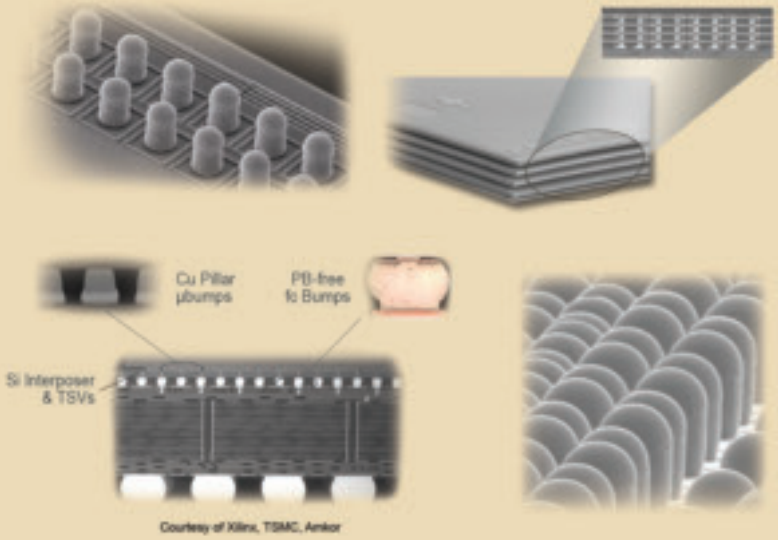
System Level Approach

- Lower cost system packaging
- Ultra-fine pitch, ultra-thin die
- Controlled stress for ULK
- 2.5D/3D Through Silicon Via (TSV) enablement
- Enhanced electromigration resistance
- Superior thermal performance
- Pb-free/Low alpha solution

With proven reliability in volume manufacturing!

Amkor Technology®

Copper Pillar μBumps



VISIT AMKOR TECHNOLOGY ONLINE FOR LOCATIONS AND TO VIEW THE MOST CURRENT PRODUCT INFORMATION.

www.amkor.com

Preceding the Device Packaging Conference...

9th Annual GBC Spring Conference and Marketing Forum

Covering the Business Side of Microelectronics Assembly and Packaging

March 10 - 11, 2013

Radisson Fort McDowell Resort and Casino

Please visit www.imaps.org/gbc to register for the GBC Conference.

Sunday, March 10

5:30 PM - 7:00 PM - Registration and GBC Welcome Reception *(Beverages and Appetizers)*
7:00 PM - 9:00 PM - Speaker's Dinner *(by Invitation)* ***Sponsored by: SSEC; Amkor Technology, ASE Group, and Kyocera***

Monday, March 11

7:00 AM - 8:00 AM - Continental Breakfast and Registration
7:00 AM - 5:00 PM - Registration

The IMAPS GBC is pleased to announce its 2013 Spring Conference. Key industry leaders will provide important information on the critical role that supply chain management plays in our global industry. Presenters will address how business models, industry collaboration, and market dynamics can have profound impacts on the increasingly interconnected semiconductor supply chains. Participants will gain valuable industry insight to achieve a competitive advantage in product development, manufacturing, marketing, and sales. The conference will facilitate networking with key decision-makers across our broad industry supply chain.

Co-Chairs: Iris Labadie, Kyocera America; Steve Annas, nMode Solutions

8:00 am - 8:15 am: Opening Remarks
Steve Annas, nMode Solutions, Inc.

8:15 am - 11:55 am: Morning Presentations
Medical Electronics Trends for Evolving Healthcare Ecosystems
Moderators: Peter Tortorici, Medtronic, Inc.;
Iris Labadie, Kyocera America

8:15 am - 9:00 am: "Medical Electronics Crossroad – from Healthcare to Health"
Keith Lindor, Arizona State University

9:00 am - 9:30 am: "Implantable Electronics Technology Needs for Improved Cost Efficient Care and Emerging Markets"
David Ruben, Medtronic, Inc.

9:30 am - 10:00 am: "Supply Chain Issues With New Electronic Packaging Technologies"
John Dzarnoski, Starkey Hearing Technologies

10:00 am - 10:20 am: Coffee Break

10:20 am - 10:50 am: "Collaborating to Compete: Biomedical Sensor Failure Prediction"
Colin Drummond, Case Western Reserve University

10:50 am - 11:20 am: "Latest Trends in Advanced Packaging Technologies and Focus on Medical Applications"
Lionel Cadix, Yole Développement

11:20 am - 11:55 am: "Opportunities for Microelectronics Packaging Technologies to Advance Wireless/Mobile Health"
Mehren Mehrgany, Case Western Reserve University

Device Packaging Welcome Reception *(GBC Attendees Invited)*
5:15 pm - 6:45 pm (Beverages and Appetizers)

Texas Hold'em Poker Tournament ***(Limited Seating)***
7:00 pm - 10:00 pm: benefits IMAPS Microelectronics Foundation

12:00 pm - 1:00 pm: Lunch & Luncheon Keynote
"The "New" IC Industry Cycle Model"
Bill McClean, President of IC Insights

1:15 pm - 5:10 pm: Afternoon Presentations
Trends in Microelectronics & Factors Shaping Enabling Technologies
Moderators: Lee Smith, Plexus Corp.;
David D'Ambra, DuPont Microcircuit Materials

1:15 pm - 2:00 pm: "Saving Lives with MEMS and Sensors: Advancements in Packaging"
E. Jan Vardaman, TechSearch International

2:00 pm - 2:30 pm: "Material Requirements for the Electronics Industry today and in the Next Decade"
Vern Stygar, AGC Electronics

2:30 pm - 3:15 pm: "Microelectronics: Driving Increased Energy Productivity"
Jeff Perkins, Energy & Resource Solutions

3:15 pm - 3:30 pm: Coffee Break

3:30 pm - 4:10 pm: "Supply Chain Eco-systems for Next Generation 3D and High-density Flip Chip Interconnection"
Jean Trewhella, IBM Corporation

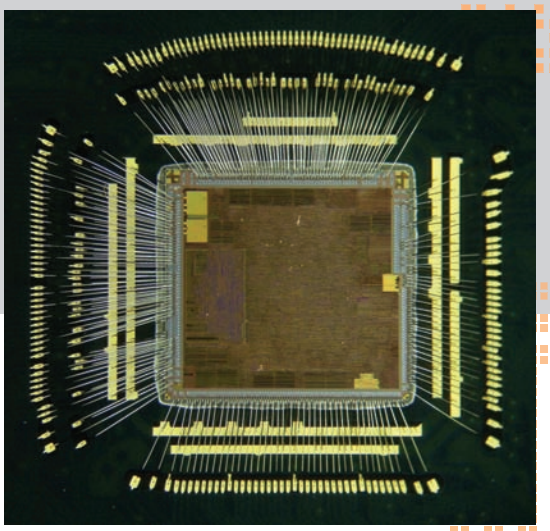
4:10 pm - 4:40 pm: "Defense Electronics Today and in the Next Decade"
Mark Darrow, Cobham Defense

4:40 pm - 5:10 pm: "Virtual Factory: Cloud Based System for Global Manufacturing & Data Management"
Simon Gonzales, Murata - RF Monolithics, Inc.

5:10 pm - 5:20 pm: Closing Remarks, Final Questions, and Conference Evaluation
Steve Annas, nMode Solutions, Inc.

ASE GROUP

Copper Wire



- Cu wire bond as good as gold
- Low cost opportunity
- Wire diameters as low as 0.7 mils
- Leader in high volume production
- Quality and yield equivalent to gold
- High reliability, typically 2x JEDEC

www.aseglobal.com

MONDAY, MARCH 11, 2013	Professional Development Courses (PDCs)				
7:00 am – 7:00 pm	**Registration**				
7:00 am – 8:00 am	**Continental Breakfast**				
8:00 am – 12:00 pm	Morning Professional Development Courses (PDCs)				
	PDC1: **2.5D/3D, Flip Chip WLP, MEMS & LED Packaging Trends, Updates & Advances** Course Leader: Phillip G. Creter, Creter & Associates	PDC2: **Recent Advances in Glass & Silicon Interposers for 2.5D and 3D Integration** Course Leader: Venky Sundaram, Georgia Institute of Technology (PRC)	PDC3: **High-Temperature Electronics - with an Emphasis on Assembly & Packaging** Course Leader: Randall Kirschman, Consultant	PDC4: **Hermetic Sealing and Testing of Small Volume MEMS Packages** Course Leader: Thomas J. Green, TJ Green Associates LLC	PDC5: **Failure Mode Analysis of Flip Chip and Advanced Package and Board Assemblies** Course Leader: Daniel Baldwin, Engent, Inc.
10:00 am – 10:20 am	**Break**				
12:00 pm – 1:00 pm	**Lunch** **Only provided for those attendees registered for both Morning and Afternoon PDCs**				
1:00 pm – 5:00 pm	Afternoon Professional Development Courses (PDCs)				
	PDC6: **Fundamentals of Glass Technology and Applications for Advanced Semiconductor Packaging** Course Leader: TJ Kiczenski, Corning, Inc.	PDC7: **Polymers for Electronic Packaging** Course Leader: Jeffrey Gotro, InnoCentrix, LLC	PDC8: **Thermal & Mechanical Simulation Techniques - An Introductory Course for 3D Enablement Professionals** Course Leader: Kamal Karimanal, Cielution LLC	PDC9: **MEMS Reliability and Packaging** Course Leader: Slobodan Petrovic, Oregon Institute of Technology	PDC10: **Basics of Conventional and Advanced Packaging** Course Leader: Syed Sajid Ahmad, Center for Nanoscale Science and Engineering, NDSU
3:00 pm – 3:20 pm	**Break**				
5:15 pm – 6:45 pm	**Welcome Reception (All Attendees "GBC & DPC" Are Invited To Attend)**				
7:00 pm – 10:00 pm	**Texas Hold'em Tournament *(Limited Seating)* - *http://www.imaps.org/DevicePackaging/holdem2013.htm*** **To Benefit the IMAPS Microelectronics Foundation**				

PDC1: 2.5D/3D, Flip Chip WLP, MEMS & LED Packaging Trends, Updates & Advances

Course Leader: Phillip G. Creter, Creter & Associates

Course Description:
This NEW overview focuses on the four technical topics of this 2013 Device Packaging Conference, independently reviewing leading edge technical developments featuring the latest in microelectronics updates/trends. Specific topics from 2012-1Q2013 conferences, technical papers, news reports:

- 2.5D/3D (Status/market, wide I/O memory stacking, polymer isolated TSVs, silicon bridge TSVs, fusion glass substrates, wafer adhesives, thin stacking, test vehicle demos, self-assembly).
- Flip Chip Wafer Level Packaging (Status/market, fine pitch copper pillars, electromigration, intermetallic compound studies, non-conductive film used in wafer level underfill, low cost FC-PoP, electromigration of lead free solder bumps).
- MEMS (Status/market, challenges, novel approaches, hermetic wafer level packaging, drop reliability, flex adhesive).
- LED Packaging (Status/market, high power heat sinks/die attach material, novel encapsulants, silicon/glass/GaN substrates).

Technical innovations related to the above topics presented with input from leading industrial/academic institutions: Advanced Semiconductor Engineering/ASE, Altera, Amkor, CEA-Leti, Corning, DELO, Georgia Institute of Technology, Global Foundries, Hitachi, Hong Kong University, IBM, IFTLE, Intel, ITRS, Karlsruhe Institute, Microsystems, NAMICS, National Tsing Hua University, Oracle, Philips Lumileds, Qualcomm, Samsung, Sandia National Labs, Sematech, Solid State Technology, Siliconware Precision Industries/SPIL, TechSearch, Tohoku University, Toray, Toshiba, University of California, Wuhan National Laboratory for Optoelectronics, Xilinx, Yole and others. Emphasis on visual aids (photos, figures, videos) with pass-around microcircuit samples. An invaluable handout includes over 100 references.

Who Should Attend?
Designed primarily for all engineers, scientists and others interested in an up-to-date overview of new developments in 3D, Flip Chip, MEMS and LED. The course uses simple terms and many graphics and figures to describe these elements of advanced packaging for those who are new to the field and needing a running start in these four focused areas of packaging technology. Ideal for entry-level technicians and engineers but also for people in quality assurance, sales, marketing, purchasing, safety, administration and program management since it also includes a short review of current single chip and advanced wafer levels of 3D packaging.

Phillip Creter is a consultant (Creter & Associates) with 30 years of microelectronics experience at Polymer Flip Chip, Mini-Systems, GTE, Itek Corporation. Past positions at GTE included Microelectronics Center Manager (received GTE Corporate Lesley Warner Technical Achievement Award), and Principal Investigator of GTE IR&D Projects. Other positions elsewhere included management in Projects/Process Engineering, Process Development, Materials Engineering/Manufacturing Engineer, receiving many awards of distinction. Creter has been teaching college-level microelectronics courses since 1997. He has continuously taught PDCs since 2004 for online webinars and national microelectronics symposia/workshops. He is a well-known presenter having published technical papers in IEEE Transactions, Solid State Technology, High Density Interconnect, Circuits Manufacturing, Insulation Circuits, others. He has chaired many technical symposia sessions, given numerous technical presentations, is a US patent-holder. He is an active certified Department of Homeland Security instructor, a Life member of IMAPS, elected Fellow of the Society, and has held several executive committee offices both locally/nationally.

PDC2: Recent Advances in Glass and Silicon Interposers for 2.5D and 3D Integration

Course Leader: Venky Sundaram, Georgia Institute of Technology (PRC)

Course Description:

This course will present a comprehensive review of the latest 2.5D and 3D interposer approaches being developed worldwide. High density interposers are emerging as a mainstream technology for packaging of heterogeneous ICs and 3D ICs, but also as a simpler and better alternative to 3D ICs with TSV, eventually providing a path for integration of sub-systems or entire systems. Silicon and glass interposers are emerging as the front-runners to address the I/O, CTE, warpage and thermal limitations of current organic packages. The topics covered include Electrical & Mechanical Design, Silicon Interposers, Glass Interposers, Chip Level & Board Level Interconnections, Applications and Markets, and Manufacturing Infrastructure for interposers. Wafer based BEOL Si interposers as well as emerging panel based glass and other interposer technologies will be described in detail. A variety of materials and process options for interposer fabrication will be presented. The technical and business challenges that must be addressed for successful implementation of interposers in 3D packages will be discussed. Specific examples of key interposer developments such as Xilinx stacked silicon interconnect, MEMS packaging using glass interposers, silicon interposer for high performance CPU packaging, and logic-memory high bandwidth 3D integration will be highlighted. For 2013, the course materials will be updated to include technology highlights in the past twelve months.

Who Should Attend?

This popular course is a must-attend event for those highly interested in interposer technology advances for the future. The course is intended for a broad audience including semiconductor and packaging managers, technologists, engineers, industry and academic researchers, and students.

Dr. Venky Sundaram is the Director of Research at the 3D Systems Packaging Research Center (PRC), Georgia Tech. He is the Program Manager for the Silicon and Glass Interposer (SiGI) industry consortium with more than 25 active global industry members. His research expertise is in the areas of System on a Package (SOP) technology, 3D packaging and integration, ultra-high density interposers, embedded components and systems integration. He is a globally recognized expert in packaging technology and a co-founder of Jacket Micro Devices, an RF/wireless start-up acquired by AVX. Dr. Sundaram is the co-chairman of the IEEE CPMT Technical Committee on Interconnections and Substrates and is on the Executive Council of IMAPS as Director of Education Programs. Dr. Sundaram has won several best paper awards and has 15+ patents and 100+ publications. He received his BS from IIT Mumbai, and MS and PhD in Materials Science and Engineering from Georgia Tech.

PDC3: High-Temperature Electronics - with an Emphasis on Assembly & Packaging

Course Leader: Randall Kirschman, Consultant

Course Description:

High-Temperature Electronics (HTE) is a valuable option for substantially improving overall system performance. Operating temperature can be an additional design parameter when justified by system performance requirements. Applications of HTE include many areas of science and technology, including petroleum and geothermal wells, vehicles, aircraft, Solar System exploration, and electric power. Relocating electronic subsystems to high-temperature can improve overall system efficiency, decrease size and weight, simplify maintenance and improve reliability. At the same time there are many technical challenges, related to materials interactions, component behavior, circuit design and interfacing. The focus of this course is semiconductor electronics assemblies at high temperatures: applications, advantages and drawbacks, technical issues and present situation. Topics include semiconductor device behavior and capabilities, packaging and assembly materials characteristics as a function of temperature, passive electronic component behavior, practical aspects of choosing packaging and assembly material and techniques. The temperature range covered in this course extends from 125°C upward, as high as 1000°C, although emphasis is on the more practical range of approximately 125°C to 300°C. The course notes include approximately 160 PowerPoint slides, more than 100 pages of detailed notes, and more than 300 references.

Who Should Attend?

Engineers and technical persons developing, designing or working with electronics for operation at high temperatures. A basic background in electronic materials and devices will be helpful.

Dr. Randall Kirschman is an internationally recognized authority on extreme-temperature electronics. He has been consulting to industry, government and academe since 1980 in the areas of micro-electronic materials and fabrication technology, and electronics for extreme temperatures. Before going into business for himself, he managed an R&D processing laboratory a division of Eaton Corporation, where he was responsible for the fabrication of microwave thin-film circuits. Prior to that he was on the staff of the Jet Propulsion Laboratory, performing research on a variety of semiconductor materials and devices. During 1990-91 he was a Visiting Senior Research Fellow at the University of Southampton, England. and between 1998-2005 was a member of the Physics Department at Oxford University. He edited the 1999 IEEE Press/Wiley book High-Temperature Electronics. He completed his undergraduate studies at the Univ. of California, and earned his Ph.D. in Physics & Electrical Engineering at the California Institute of Technology.

PDC4: Hermetic Sealing and Testing of Small Volume MEMS Packages

Course Leader: Thomas J. Green, TJ Green Associates LLC

Course Description:

Reliable packaging of MEMS requires the ability to create and maintain a suitable inert atmosphere or vacuum inside the package cavity for the expected lifetime of the device. Traditional hermetic ceramic/metal packages are being replaced by wafer level packaging techniques, which present unique challenges from a hermeticity testing perspective. This course begins with an overview of traditional hermetic sealing processes along with wafer level MEMS packaging processes and methods. In some cases near-hermetic packages, such as LCP are suitable for some applications. Testing of small cavity MEMS packages according to the traditional Mil Spec TM 1014 requirements may not be sufficient to guarantee reliable operation. Difficulties and limitations in fine leak testing of small volume packages will be addressed. Recent advances in Optical Leak Testing (OLT), Cumulative Helium Leak Detection (CHLD) along with other hermeticity techniques, such as pirani vacuum sensors, are reviewed in light of the new tighter hermeticity specifications. Gaseous ingress is of primary concern for a small volume MEMS cavity packages. Moisture level vs. surface area to volume ratio is an important concept, along with material outgassing and the potential to mitigate these problems with getters. These along with other critical MEMS packaging issues are addressed.

Who Should Attend?

This PDC is intended as an intermediate level course for process engineers, designers, quality engineers, and managers responsible for packaging and hermetic testing of small volume cavity style packages.

Thomas J. Green is the principal at TJ Green Associates LLC (www.tjgreenllc.com), a veteran owned small business specializing in teaching and consulting for the microelectronics industry. Tom has demonstrated expertise in sealing and hermeticity testing of products intended for high rel military and medical applications. He is currently on the JEDEC committee helping to revise TM 1014 and has served as an expert witness in medical cases related to hermeticity failures. Tom is an active member of IMAPS and a Fellow of the Society. He has a B.S. in Materials Engineering from Lehigh University and a Masters in Engineering.

PDC5: Failure Mode Analysis of Flip Chip and Advanced Package and Board Assemblies

Course Leader: Daniel Baldwin, Engent, Inc.

Course Description:

Over the past few years, numerous advanced packaging and process technologies have emerged such as flip chip in package, PoP, SiP, WLCSP, 3D-WLCSP, QFN, etc.. While a large number of technical publications are available to help with process requirements, understanding failure modes and reliability standards is essential for these technologies to be successfully sustained in production. This course will present reliability test procedures, assembly process defects, and common failure modes that occur in advanced package and board level assemblies. It will focus on process defect identification and resolution, failure mechanisms and the associated analysis tools needed to identify them such as FTIR, XRF, transmission X-ray analysis, acoustic microscopy and scanning electron microscopy. Numerous process defects and failure modes will be presented along with extensive visual aids to provide a more intuitive understanding of the defects and failure modes associated with these advanced assemblies. It will also discuss artifacts leading to process defects and how they can contribute to premature failure.

Who Should Attend?

Individuals associated with electronics packaging, package reliability, package failure analysis, and assembly process control/defects are encouraged to attend. The following are encouraged to attend. Managers. Knowledge gained through this course will allow managers to make informed decisions about the technical feasibility, implementation factors, performance benefits, reliability, and risks of implementing flip chip technology. Engineers. Manufacturing, quality, design, and packaging engineers in integrated circuit, equipment, materials, and system design who are challenged to solve process defects and packaging problems. Knowledge gained through this course will allow engineers and technologists to make informed decisions about the technical feasibility, implementation factors, performance benefits, reliability, and risks of implementing flip chip technology.

Dr. Daniel F. Baldwin is the President and CEO of Engent, Inc.-Enabling Next Generation Technologies providing enabling manufacturing services and process technologies in the areas of microelectronics, flip chip, optoelectronics, and MEMS. He is one of the 2003 founding partners of Engent. He recently completed an Adjunct Associate Professor of Mechanical Engineering position at the Georgia Institute of Technology. He was a tenured Associate and Assistant Professor of Mechanical Engineering at Georgia Tech from 1995 through 2005. At Georgia Tech, he headed the Low Cost Flip Chip Processing program for the Packaging Research Center, the Advanced Interconnect Technologies research program for the Manufacturing Research Center, and the Low Cost Assembly Processing Program for the CBAR. Prior to joining the faculty, he was a Member of the Technical Staff at Bell Laboratories, Princeton NJ working on electronic product miniaturization. He was formerly the Vice President of Siemens' Advanced Assembly Technology Division. He also served as a research manager and research assistant at MIT's Laboratory for Manufacturing and Productivity from 1990 to 1994, a Draper Fellow at the Charles Stark Draper Laboratory in Cambridge MA from 1988 to 1990, and an Engineering Intern for Mitsubishi Electric, Kamakura, Japan in 1987. Dr. Baldwin received his S.M. and Ph.D. degrees in Mechanical Engineering from MIT in 1990 and 1994, respectively. Dr. Baldwin served as the Technical Program Chair of the IMAPS 2nd International Advanced Technology Workshop on Flip Chip Technology and the General Chair of the IMAPS 3rd International Advanced Technology Workshop on Flip Chip Technology. Dr. Baldwin was the recipient of the ASME Electrical and Electronics Packaging Division's Outstanding Young Engineer Award, 1998 and the Milton C. Shaw Outstanding Young Manufacturing Engineer Award, Society of Manufacturing Engineers, 1999. He has sixteen years of experience in the electronics manufacturing and packaging industries, eight U.S. Patents, over 230 scholarly publications, and expertise in electronics packaging, MEMS packaging, advanced materials processing and manufacturing systems design. Dr. Baldwin is a past President of the Surface Mount Technology Association (SMTA), and formerly on the Board of Advisors for the Society of Manufacturing Engineers/Electronics Manufacturing Division (SME/EM). He was on the editorial advisor board of Advanced Packaging magazine and HDI magazine. He is on the Board of Directors of Engent, Inc. and Akrometrix, LLC, and the Board of Advisors for IC Interconnect. Dr. Baldwin was also on the technical Board of Advisors of RFIDentics Corp. which was acquired by Avery Dennison Corp.

PDC6: Fundamentals of Glass Technology and Applications for Advanced Semiconductor Packaging

Course Leader: TJ Kiczenski, Corning, Inc.

Course Description:
The objective of this course is to build a foundation of understanding of engineered glass as a material that technologists can leverage in the development of advanced IC packaging applications. Starting from the fundamental principles of glass structure, composition and properties we will provide a broad overview of glass with a focus on unique attributes that make glass as an enabling material. Subjects to be covered will include strength and reliability, chemical durability, thermal behavior, associated thermal relaxation behavior, and electrical properties. Additionally we will review the platform alternatives as part of the "glass toolkit" available to semiconductor packaging development including various manufacturing (melt & form) approaches, the diversity of compositional options and a survey of glass processing options that can be adapted from adjacent glass technology space to advanced semiconductor packaging. Finally the course will illustrate with case studies how glass is contributing to emerging 3D-IC technologies and explore current and potential applications in advanced semiconductor packaging. We will focus on its role as a carrier for temporary bonding, integrated wafer for CMOS Image Sensor, and 2.5D and 3D glass interposers. Relative costs of glass will be discussed as an alternative to other materials for carriers and interposers.

Who Should Attend?
The target audiences include individuals or companies with little or no experience in using glass. Engineers, technical managers, scientists, buyers, and managers involved in materials, research and development, and 3D IC packaging.

Dr. TJ Kiczenski is a Research Associate with Corning Incorporated. His work includes investigations of the physics of glass relaxation, liquidus relationships in multicomponent glass forming systems, metallic glasses, and glass/glass and glass/ceramic composite materials. He is credited as the inventor or co-inventor of several Corning Display Technology products manufactured by the proprietary fusion process, including Corning Lotus Glass for low-temperature polysilicon display applications. He received his PhD in Geology and M.S. in Materials Science from Stanford University where he investigated the structure of fluorine in silicate and aluminosilicate glasses and his B.A. degree in Physics from Coe College where he studied alkali-germanate glasses. Aric Shorey, PhD, is a Sr. Technical Manager at Corning Incorporated working on the Semiconductor Glass Wafer program. He has BS/MS in Mechanical Engineering and a PhD in Materials Science - all from the University of Rochester. He has spent the majority of his career in material's finishing and characterization for the telecommunications, precision optics and semiconductor industries.

PDC7: Polymers for Electronic Packaging

Course Leader: Jeffrey Gotro, InnoCentrix, LLC

Course Description:
This course will provide a broad overview of polymers and the important structure-property-process-performance relationships for electronic packaging. Topics to be covered are thermosetting polymers versus thermoplastics, thermosetting polymer curing, curing mechanisms (heat and light cured), network formation, and an overview of key chemistries used (epoxies, acrylates, polyimides, bismaleimides, curing agents, and catalysts). The course will provide a more in-depth discussion of the chemistries, material properties, and process considerations for adhesives (both paste and film), capillary underfills, packaging substrate materials, encapsulants (mold compounds), and coatings. In most cases, adhesives, underfills, mold compounds and coatings are applied as a viscous liquid and then cured. The flow properties are critical to performance in high volume manufacturing. The final portion of the PDC will provide an introduction to rheological characterization methods (various types of rheometers and viscometers) and the properties of adhesives (shear thinning, viscosity, time dependence, rheology changes during curing), underfills, and mold compounds.

Who Should Attend?
Packaging engineers and R&D professionals involved in the development, production, and reliability testing of semiconductor packages would benefit from the course.

Dr. Jeffrey Gotro has over twenty-six years experience in polymers for electronic applications and composites having held scientific and leadership positions at IBM, AlliedSignal, Honeywell, and Ablestik Laboratories. He is an accomplished technology professional with demonstrated success solving complex polymer problems, directing new product development, and enabling clients to improve the financial impact of their polymer technologies. Jeff has consulting experience with companies ranging from early-stage start-ups to Fortune 50 companies. Jeff is a nationally recognized authority in thermosetting polymers and he has received invitations to present lectures and short courses at national technical conferences. He has published 60 technical papers (including 4 book chapters) in the field of polymeric materials for advanced electronic packaging applications, holds 13 issued US patents, and has 8 patents pending. Jeff has a Ph.D. in Materials Science from Northwestern University with a specialty in polymer science and a B.S. in Mechanical Engineering/Materials Science from Marquette University.

PDC8: Thermal and Mechanical Simulation Techniques - An Introductory Course for 3D Enablement Professionals

Course Leader: Kamal Karimanal, Cielution LLC

Course Description:
The industry is becoming increasingly aware of the fact that thermal and mechanical factors are crucial hurdles to the realization of TSV based 3 Dimensionally stacked IC products. These challenges are pervasively felt at all stages of the product development cycle starting from Layout, IC design, power management, assembly processing strategy, package design, and testing. Due to the need to narrow down from a myriad of costly choices even prior to test chip or prototype development, engineering simulation is an important tool at the disposal of the engineer. As a result, engineers from all IC design and packaging background who are tasked with the responsibility of enabling 3D ICs are interested in utilizing thermal and mechanical simulation. This is an introductory course on thermal and mechanical simulation techniques pertaining to 3D Through Silicon Stacking meant for engineering professionals involved in the enablement of TSV based 3D stacked SOCs. Thermal Modeling Techniques: Steady-State, Transient, Detailed and Compact. Modeling Tools and Techniques for 3D IC Thermal Management. Overview of mechanical challenges to 3D stacking: warpage, assembly Yield, CPI effects on Yield & reliability Mechanical Modeling Tools and Techniques for Technology development and Reliability. Mobility/stress distribution: Contributions from package, TSV and devices.

Who Should Attend?
Any Engineering professional involved in 3D enablement with interest in the Thermal and mechanical challenges. Also suited for technologists and managers interested in deploying engineering simulation as a strategic tool for understanding thermo-mechanical feasibility, risks and benefits of costly technological investments related to 3D TSV based products.

Kamal Karimanal is the Founder of Cielution LLC, which is an engineering simulation software and services company serving the electronics supply chain. Prior to starting Cielution, Dr. Karimanal has served in several engineering simulation focused roles at Fluent Inc, ANSYS Inc and Globalfoundries. Dr. Karimanal has contributed to several detailed and compact modeling methodologies which are being widely used by the electronics industry today. He has written several conference and journal papers and online application notes. Dr. Karimanal received his Ph. D in Mechanical Engineering from The University of Texas at Austin.

PDC9: MEMS Reliability and Packaging

Course Leader: Slobodan Petrovic, Oregon Institute of Technology

Course Description:

This course provides a comprehensive discussion of a broad array of MEMS packaging and reliability issues. An overview of the principles of operation, fabrication methods, and materials used in building MEMS structures will be presented as well. Because each MEMS device requires a distinctive packaging approach, practical examples and illustrations will be used to demonstrate uniqueness of solutions and interactions between micromachined structures and packaging. A full range of MEMS devices will be discussed while a particular emphasis will be placed on sensors and actuators used in industrial, medical, and automotive applications. Extensive case studies that will be used to most effectively demonstrate diverse packaging principles for devices such as accelerometers, pressure sensors, and digital micromirror devices. The course will be divided in 2 major sections: general MEMS competence; and packaging and reliability. The following major topics will be covered: fabrication technologies, materials, design and device physics, main MEMS types, integration aspects, selected industrial application, design considerations, types of packaging, quality control, reliability and failure analysis.

Who Should Attend?

While some prior knowledge by the participants of MEMS in general is helpful, the packaging discussion will include a detailed explanation of the principles of operation, fabrication methods, and materials used in building MEMS structures. The course is therefore open to participants with no prior MEMS knowledge and would provide a reasonably broad general introduction into the field. The participants will have the opportunity to gain knowledge about MEMS in general through the eyes of a packaging and reliability specialist.

Dr. Slobodan Petrovic is an associate professor at the Oregon Institute of Technology in Portland, OR. His research interests are in the areas of MEMS fuel cells, sensor media compatibility, hydrogen generation and storage, and dye-sensitized solar cells. Prior to that, he was at the Arizona State University, where he taught courses in MEMS, Sensors, and alternative energy. Dr. Petrovic also held appointments at Clear Edge Power as a Vice President of Engineering; at Neah Power Systems as Director of Systems Integration; and Motorola, Inc. as a Reliability Manager. Dr. Petrovic has over 25 years of experience in MEMS, sensors, energy systems; fuel cells and batteries; and electrochemical solar cells. He has over 50 journal publications and conference proceedings; 2 book contributions and 24 pending or issued patents.

PDC10: Basics of Conventional and Advanced Packaging

Course Leader: Syed Sajid Ahmad, Center for Nanoscale Science and Engineering, NDSU

Course Description:

The course presents manufacturing, materials, quality and reliability info in terms understandable to engineering and non-engineering personnel. Packaging characteristics and drivers will be outlined. Types of packages and critical differences among them and their applications will be discussed. The course will look at the design selection to meet use and application environments. Step-by step manufacturing flow for plastic packages will be presented as an example to understand the complexity of processes, materials and equipment involved in their manufacture. Advanced packaging will be introduced. Materials selection with respect to application environments will be discussed. Quality and reliability issues related to chip packaging and SMT and their solution will be outlined. Topics: Packaging characteristics and drivers. Types of packages and critical differences among them. Design selection to meet use and application environment. Step-by step manufacturing flow for plastic packages. Advanced packaging. Materials selection. Quality and reliability issues.

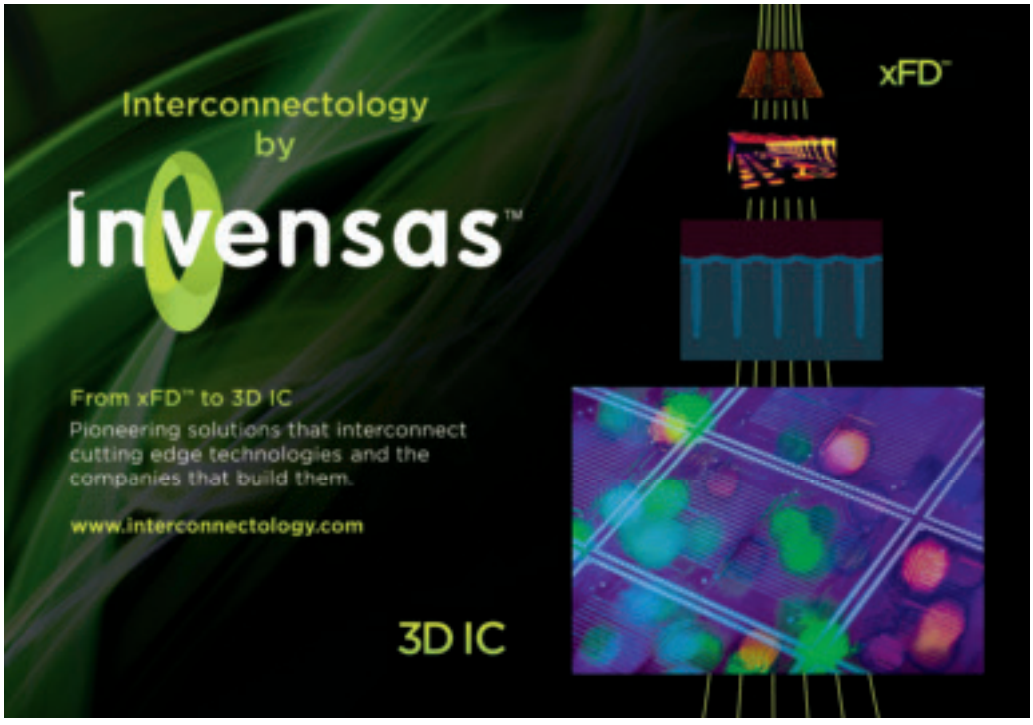
Who Should Attend?

It will help the attendees understand the effects of package configurations on their work and the effect of their work on chip packages. Personnel entering the packaging field will have a critical look at the quality, reliability and materials issues related to the development and manufacture of chip pacakages. Non-packaging personnel will learn ins and outs of chip packaging. Non-technical personnel will learn the material and manufacturing intricacies of simple looking chip packages.

Syed Sajid Ahmad contributed to quality and reliability enhancement of assembly processes at Intel (1979-89), especially wire bond. Ahmad also contributed to packaging development at National Semiconductor (1990) and managed quality at GigaBit/TriQuint (1990-91). His major work at Micron Technology (1991-2003) involved the development and implementation of advanced packaging. At the Center for Nanoscale Science and Engineering, Ahmad's focus is on enhancing research and manufacturing capabilities in the areas of thin film, thick film, chip scale packaging (CSP) and surface mount technology (SMT). Ahmad has 34 international publications & presentations and holds 54 patents.

DPC/GBC Premier Sponsors:		
SSEC	Amkor Technology	ASE GROUP
Event Sponsor - Exhibit Reception, Lunch & Break: APPLIED MATERIALS	**Post-Conference Presentations USB Drives:** ALLVIA	**Conference Badge Lanyards:** NAMICS
3D Panel Discussions: invensas	**Refreshment Breaks:** SIKAMA Reflow Solder Systems	**Refreshment Breaks:** STATSChipPAC
Refreshment Breaks: SETNA	**GBC Speaker Dinner:** SSEC	**GBC Speaker Dinner:** Amkor Technology
GBC Speaker Dinner: ASE GROUP	**GBC Speaker Dinner:** KYOCERA	

Media Sponsors:			
3DInCites.com	3D Packaging	Micronews	MEPTEC



TUESDAY, MARCH 12, 2013 — Morning Technical Sessions

7:00 am – 7:00 pm	**Registration**
7:00 am – 8:00 am	**Continental Breakfast**
8:00 am – 8:20 am	**OPENING COMMENTS**
8:20 am – 9:05 am	**KEYNOTE – 3D Packaging** ***2.5 and 3D - Scaling Walls*** *Dr. Sitaram R. Arkalgud, Vice President of 3D Technology* INVENSAS CORPORATION **Abstract**: Stacking chips, either on a 2.5D interposer or in true 3D ICs, is an industry game changer since it promises the benefits of higher performance, functionality and density at lower power consumption. With advent of the first 2.5D products in volume production, the need to reduce cost, particularly for consumer applications, is gaining prominence. Lithographic scaling has driven performance and cost vectors in the semiconductor industry for decades. Comprehensive models, developed to understand the impact of scaling on device performance, reliability and cost, make it easier to develop scaling roadmaps. In a similar fashion, credible models for 3D interconnects are critical, since these will underpin the development of future 3D technology "nodes" by providing performance and cost estimates. The roadmaps, in turn, will drive the development of materials, equipment, EDA tools and products. This presentation will examine some of the near term manufacturability concerns as well as key areas for 3D scaling, together with the electrical and thermo-mechanical challenges that accompany them. ***Dr. Sitaram R. Arkalgud*** *is Vice President of 3D Technology at Invensas Corporation, a complete Interconnectology solutions provider for advanced mobile applications. Previously, Arkalgud started and led 3D IC development at SEMATECH, where the focus was on delivering manufacturable process technologies for 3D interconnects. In addition, he has worked in a variety of roles spanning R&D and manufacturing in memory and logic technologies at Infineon/Qimonda and Motorola. Arkalgud holds a doctorate and master's degree in materials engineering from Rensselaer Polytechnic Institute in Troy, NY, and a bachelor's degree in metallurgical engineering from Karnataka Regional Engineering College, Suratkal, India. He is the author of several publications and holds 14 U.S. patents.*
9:10 am – 9:55 am	**KEYNOTE – Flip Chip & Wafer Level Packaging** ***Semiconductor Packaging Trends and Materials Challenges*** *Dr. Mahadevan "Devan" Iyer, Director of Worldwide Semiconductor Packaging operations* TEXAS INSTRUMENTS **Abstract**: Semiconductor advancements continue to enable many new applications to enable the Internet of Things, and transform areas such as cloud computing, health care, safety and security, and consumer electronics. As exciting new capabilities emerge, customers are demanding smaller, thinner, faster and more power efficient solutions. In his keynote presentation, Dr. Mahadevan "Devan" Iyer will discuss these trends, and how packaging technology is playing an increasingly important role in delivering these benefits in IC products. Dr. Iyer will outline the materials requirements and challenges for increased electrical, thermal and reliability performance. *As Director of TI's Worldwide Semiconductor Packaging operations,* ***Dr. Mahadevan "Devan" Iyer****, oversees a global team that drives a process to determine the packaging design and technologies that best meet the requirements of our customers in measures of miniaturization, performance cycle time, and cost. Dr. Iyer joined TI in 2008 to lead the global SC Packaging team. He has more than 25 years of experience in the microelectronics industry. Dr. Iyer is a recognized authority in semiconductor packaging technologies. He has more than 150 technical publications and 28 patents to his credit.*
10:00 am – 10:30 am	**Break in Exhibit Hall**
10:00 am – 7:00 pm	**Exhibition and Technology Showcase**

	Advanced 3D Packaging	**Flip Chip & Wafer Level Packaging**	**MEMS & Microsystems**
	TA1: **3D Packaging Applications** Chairs: Peter Ramm, Fraunhofer EMFT; Franck Murray, IPDIA	TA2: **Flip Chip & Cu Pillar Assembly Reliability** Chairs: Andrew Strandjord, Pac Tech-USA Alan Huffman, RTI International	TA3: **MEMS Devices and Processes** Chairs: Tracy Hudson, U. S. Army AMRDEC; Philip Reiner, CGI Federal Systems
10:30 am – 11:00 am	Cost Drivers for 2.5D and 3D Applications Chet Palesko, SavanSys Solutions LLC (E. Jan Vardaman TechSearch International, Inc.; Alan Palesko, SavanSys Solutions LLC)	Reliability of Die to Wafer Bonding Using Copper-Tin Interconnections Arnaud Garnier, CEA-LETI, MINATEC (Rémi Franiatte David Bouchu, Romain Anciant, Séverine Chéramy)	Control Strategies and Trade-Offs for Micromachined Vibratory Gyroscopes with High Quality Factors Igor Prikhodko, University of California, Irvine (Alexander Trusov, Andrei Shkel)
11:00 am – 11:30 am	Stacked 3d Package with Improved Bandwidth and Power Efficiency Dev Gupta, APSTL LLC	Thermal Modeling Approach for Enhancing TCNCP Process for Manufacturing Fine Pitch Copper Pillar Flip Chip Packages Siddharth Bhopte, Amkor Technology (Jesse Galloway, Kyung-Rok Park, Hyun-Jin Park, Jeong-Han Choi, Ho-Beob Yu, Sung-Hwan Yang)	MEMS Parallel Plate Actuator Pull-in Detection and Mitigation Colin Stevens, Auburn University (Robert Dean)
11:30 am – 12:00 pm	ChipsetT: Embedded Die Substrate Applications Jon Aday, FlipChip International, LLC (Ted Tessier, FlipChip International; Kazuhisa Itoi, Satoshi Okude, Fujikura Ltd.)	Groove Geometry and Mold Shrinkage Effects on Die Stress in Flip Chip Molded BGAs (FCMBGA) Bora Baloglu, Amkor Technology (Miguel Jimarez Ahmer Syed)	Design, Simulation and Testing of High Density, High Current Micro-machined Embedded Capacitors Aubrey Beal, Auburn University (C. Stevens, T. Baginski, M. Hamilton, R. Dean)
12:00 pm -12:30 pm	Integration of Passive Components into 3D PoP Fan-Out Packages Tom Strothmann, STATSChipPAC		Flip-Chip Bonding of Au-Au MEMS Joe Sanford, UTARI - University of Texas Arlington Research Institute (Dan Popa)
12:30 pm – 2:00 pm	**Lunch Break in Exhibit Hall** (Food served from 12:30 pm - 1:30 pm)		

Exhibition and Technology Showcase:

Tuesday, March 12th
10:00 am - 7:00 pm

Wednesday, March 13th
12:30 pm - 4:30 pm

TUESDAY, MARCH 12, 2013 — Afternoon Technical Sessions

	Advanced 3D Packaging	Flip Chip & Wafer Level Packaging	MEMS & Microsystems
	TP1: **2.5D Interposer Packages** Chair: Cristina Chu, TEL NEXX; Alan Huffman, RTI International	TP2: **Topics in Bump and Die Interconnect** Chairs: Gilles Poupon, LETI; Luu Nguyen, Texas Instruments	TP3: **MEMS Packaging and Testing** Chairs: Russell Shumway, Amkor Technology; Robert Dean, Auburn University
2:00 pm - 2:30 pm	Assembly Challenges and Learnings for Large 2.5D TSV Products Michael Kelly, Amkor Technology (Marnie Mattei, Rick Reed)	Development of Plating Process for Micro Bump Formation Takuma Katase, Mitsubishi Materials Corporation (Koji Tatsumi, Tekeshi Hatta, Masayuki Ishikawa, Akihiro Masuda)	Sealing Dispensing Requirements to Meet MEMS Packaging and Throughput Impact Heakyoung Park, Nordson ASYMTEK
2:30 pm - 3:00 pm	3D Integration of System-in-Package (SiP): Toward SiP-Interposer-SiP for High-End Electronics Rabindra Das, Endicott Interconnect Technologies, Inc. (Frank Egitto, Steven Rosser, Erich Kopp, Barry Bonitz)	Production of Uniform Dimension Copper Pillars for Flip Chip CSP Stephen Kenny, Atotech Germany (Kai Matejat, Carsten Schauer, Sven Lamprecht)	Microfluidic Technology Using SU8 on Top of PCBs Stefan Gassmann, University of Rostock (Lienhard Pagel)
3:00 pm – 3:30 pm	Novel Low-Loss Photodefined Electrical TSVs for Silicon Interposers Paragkumar Thadesar, Georgia Institute of Technology (Muhannad Bakir)	Development of Thick Resist for Bumping Jim Chung, JSR Micro, Inc.	Characterization of Aluminum-Germanium Wafer Bonding for MEMS Packaging Sumant Sood, SUSS MicroTec (Robert Hergert, Oliver, Oliver Treichel, Sean Peng, Mars Chuang)
3:30 pm – 4:15 pm	**Break in Exhibit Hall**		
4:15 pm - 4:45 pm	Polymer Based Interposer with Si Matched CTE Karen Shrier, Electronics Polymer Newco Inc	Semiconductor Fluxes for Wafer Bumping in 3D Assembly Maria Durham, Indium Corporation (Laura Mauer, Solid State Equipment Corp.; Andy Mackie, Indium Corporation)	CoC (Chip on Chip) or FtoF (Face to Face) - PossumTM Technology for 3D MEMS and ASIC Eliminating the Need of TSV or Wire Bonding Jemmy Sutanto, Amkor Technology (D. H. Kang, J. H. Yoon, K. S. Oh, Michael Oh, Amkor Technology Korea; R. Lanzone, R. Huemoeller, Amkor Technology)
4:45 pm – 5:15 pm	Ultra High Density Capacitors Merged with Through Silicon Vias to Enhance Performances. Catherine Bunel, IPDIA	Fabrication of Double-Helix Contacts: Compliant Interconnect Structures for Reworkability Alexander Pfeiffenberger, Auburn University (Michael Hamilton)	Package Level Self-Test System for Electronic Compass Dario Paci, STMicroelectronics
5:15 pm – 5:45 pm	3D Packaging- Through Glass Vias TGV with Alkali Free Glass for Advanced Packaging Vern Stygar, AGC (Tim Mobley, Shintarou Takahashi)	Micro-tube Insertion into Aluminum Pads: Simulation and Experimental Validations Alexis Bedoin, CEA- LETI, MINATEC (B. Goubault de Brugiere, F. Marion, F. Berger, M. Fendler, M. Volpert, H. Ribot)	A Design Tool Fully Adapted to the Development of the Thin Film Encapsulation Used for MEMS Devices Souchon Frederic, CEA-LETI, MINATEC (Gervais Anne-Charlotte, Thouy Laurent, Saint-Patrice Damien, Pornin Jean Louis)
5:45 pm – 7:00 pm	**Reception in Exhibit Hall**		
7:00 pm – 8:30 pm	**Panel Discussion: Flip Chip & Wafer Level Packaging** **Moderator: Linda Bal, Freescale; Luu Nguyen, Texas Instruments** **Panel Members:** Miguel Jimarez, Amkor Technology, Inc.; John Hunt, ASE USA; Raj Pendse, STATSChipPAC; *Additional panelists to be announced soon*		

A SPECIAL THANKS
TO THE DEVICE PACKAGING SPONSORS!
YOU ARE THE "*GAS*" FOR THE IMAPS ENGINE!

WEDNESDAY, MARCH 13, 2013 — Morning Technical Sessions

7:00 am – 6:00 pm	**Registration**
7:00 am – 8:00 am	**Continental Breakfast**
8:00 am – 8:45 am	**KEYNOTE – MEMS** ***MEMS and MEMS Packaging for High Temperature and Other Harsh Environments*** *Dr. F. Patrick McCluskey, Associate Professor* UNIVERSITY OF MARYLAND **Abstract**: Recent advances in Microelectromechanical systems (MEMS) technology have resulted in relatively low cost MEMS gyroscopes. Their unique features compared to macro-scale devices have made them popular in many applications. Nowadays, MEMS gyroscopes are lighter, smaller and consume less power and therefore, are considered to be the best low-cost solution compared to spinning disk or wheel type mechanical gyroscopes. These low-cost MEMS gyroscopes have opened up a wide variety of applications with environmental conditions ranging from mild-to-harsh. Many of these harsh environments include high temperature, high humidity, high-G mechanical shock/drop, high-frequency mechanical vibration and high frequency acoustic noise. This web seminar will review the studies conducted to understand the effect of such harsh environment on MEMS gyroscopes. It also examines the effects of an elevated temperature and sustained exposure to temperature combined humidity on the MEMS vibratory gyroscope. ***Dr. Patrick McCluskey*** *is an Associate Professor of Mechanical Engineering at the University of Maryland, College Park. He is associated with the CALCE center where he is the principal investigator for projects related to packaging and reliability of electronic components for high power and high temperature environments. He is the author or co-author of over 100 technical articles on his research, and the co-author of three books. He has served as the technical program chair for several symposia and conferences in these research areas. He is a fellow of IMAPS and is a member of ASME, IEEE, and SAE.*
8:45 am – 9:30 am	**KEYNOTE – LEDs** ***Packaging Innovation: The Key to the Future of Solid State Lighting*** *Robert F. Karlicek, Jr., Professor & Director, Smart Lighting Engineering Research Center* RENSSELAER POLYTECHNIC INSTITUTE **Abstract**: LED technology development has progressed very rapidly since the first lighting class blue LEDs were introduced more than 20 years ago. Today, LED chip performance for solid state lighting is closing in on theoretical limits of performance and high volume manufacturing of LED devices for solid state lighting is rapidly driving down die prices. Increasingly, barriers to delivering cost effective high performance solid state lighting are driven by the limitations of conventional LED packaging technologies where optical management adds complexity to conventional packaging methods and the limitations of conventional pick and place technology add barriers to cost reduction. New approaches to LED packaging are borrowing tricks from state-of-the-art silicon device packaging methods, and continued packaging innovation is required to realize the full potential of solid state lighting. This talk reviews the status of LED lighting from the chip, packaging and lighting system perspective, and describes some key areas where packaging innovation is still required to drive adoption of solid state lighting systems. ***Dr. Robert F. Karlicek, Jr.*** *is the Director of the Smart Lighting Engineering Research Center at Rensselaer Polytechnic Institute, an NSF and industry funded program exploring advanced applications for next generation solid state lighting systems. Prior to joining RPI, he spent over 30 years in industrial research and R&D management positions with corporations including AT&T Bell Labs, EMCORE, General Electric, Gore Photonics, Microsemi, Luminus Devices and SolidUV. Dr. Karlicek is well known globally as an LED industry expert, and is a frequent presenter at conferences and workshops. He obtained his Ph.D. in Physical Chemistry from the University of Pittsburgh and has over 40 published technical papers and 26 U.S. patents.*
9:30 am – 10:00 am	**Break in Foyer**

	Advanced 3D Packaging	**Flip Chip & Wafer Level Packaging**	**LED Packaging for Future Solid-State Lighting**
	WA1: **Substrates & Materials for 3D IC Processing** Chairs: Jeff Calvert, Dow Chemicals; Phil Garrou, Microelectronic Consultants of NC	WA2: **Substrate Effects and Materials** Chairs: Lars Boettcher, Fraunhofer IZM; Linda Bal, Freescale	WA3: **Packaging for Advanced LED SSL Systems** Chairs: Thomas Goodman, E&G Technology Partners; Bob Karlicek, Rensselaer Polytechnic Institute
10:00 am - 10:30 am	Precision Glass Carriers and Metrology for Wafer Thinning Operations Aric Shorey, Corning Inc. (Bor-Kai Wang, Joe Canale, Windsor Thomas)	Effect of Substrate Layer Variation on Package Warpage Brendan Wells, Amkor Technology (Wei Lin, HyunJin Park)	LEDs for SSL - Market Trends, Drivers, and Applications Vrinda Bhandarkar, PennWell / Strategies Unlimited
10:30 am - 11:00 am	Temporary and Permanent Adhesives for Thin Wafer Handling and Assembly Mark Oliver, Dow Electronic Materials (Jong-Uk Kim, Zidong Wang, Janet Okada, Elissei Iagodkine, Anupam Choubey, Ed Anzures, David Fleming, Avin Dhoble, Chi Truong, Michael Gallagher; Kai Zoschke, Matthias Wegner, Michael Töpper, Fraunhofer IZM)	From Mechanical Adhesion to Chemical Adhesion: Challenges in Obtaining Sufficient Adhesion Between Electroless Copper and Dielectrics Robin Taylor, Atotech USA (Meng Hsieh, Ellina Libman, Lutz Brandt)	A Solder Joint Reliability Model for the Philips Lumileds LUXEON Rebel LED Carrier Using Physics of Failure Methodology Greg Caswell, DfR Solutions (Rudi Hechfellner, Michiel Kruger, Tewe Heemstra, Philips Lumileds; Nathan Blattau, Gregg Kittlesen, Vikrant More, DfR Solutions)
11:00 am - 11:30 am	Versatile Z-Axis Interconnection for High Performance Electronics Rabindra Das, Endicott Interconnect Technologies, Inc. (J. M. Lauffer, F.D. Egitto)	Adopt advanced RDL Rule to Apply Flip Chip Packaging for Next Generation Si Technology: Feasibility Study Shengmin Wen, Amkor Technology (KyungRok Park, Patrick Thompson, JeongSeok Lee, HyunJin Park)	Lithography for Wafer Level Packaging for LED Manufacturing Michael Hornung, SUSS MicroTec Lithography GmbH
11:30 am - 12:00 pm	Electrografted Insulator Layer as Copper Diffusion Barrier for TSV Interposers Vincent Mevellec, ALCHIMER (Dominique Suhr, Thomas Dequivre, Frederique Raynal)	Direct Palladium-Gold on Copper as a Surface Finish for Next Generation Packages Mustafa Özkök, Atotech (Sven Lamprecht, Gustavo Ramos, Arnd Kilian)	Advanced Passive Thermal Management for LED Bulb Systems James Petroski, Rambus
12:00 pm - 12:30 pm	Wafer Level Interconnects for 2.5D/3D Enroute to Manufacturing Sesh Ramaswami, Applied Materials		
12:30 pm – 2:30 pm	**Lunch in Exhibit Hall** (Food served from 12:30 pm - 1:30 pm)		
12:00 pm – 4:30 pm	**Exhibition and Technology Showcase**		

Post-Conference Presentations USB Drives Sponsor:	Conference Badge Lanyards Sponsor:	3D Panel Discussion Sponsor:
ALLVIA	NAMICS	invensas

WEDNESDAY, MARCH 13, 2013

Interactive Poster Sessions in Exhibit Hall

2:00 pm - 4:30 pm *(Poster setup: 1:30 pm to 2:00 pm)*

Posters

Development of Embedded High Power Electronics Modules for Automotive Applications
Lars Boettcher, Fraunhofer IZM (S. Karaszkiewicz, D. Manessis, A. Ostmann)

Development of Substrate Embedded Magnetics for DC-DC Buck Converters
Jeff Aggas, Auburn University (Aubrey Beal, Robert Dean)

Singulation Blades and Physics
Edward Perry, Kim & Ed PTE LTD Singapore

A Novel Silicone Material for 3D Flex Package with Multi Chips
Bo Zhang, Institute of Microelectronics Chinese Academy of Sciences (Wen Yin, Yuan Lu, Liao Anmou, Du Tianmin, Dongkai Shangguan, Lixi Wan)

IMAPS Microelectronics Foundation Spring Golf Invitational

Benefits the IMAPS Microelectronics Foundation

Thursday, March 14, 2013 | 1:15 pm - 7:00 pm

1:15 pm Shotgun Start - *"Best Ball" Scramble*

Desert Canyon Golf Club (www.desertcanyongolf.com)

Separate Registration - Sign up today: **www.imaps.org/DevicePackaging/golf2013.htm**

Foundation Golf Chair: David Virissimo, Coining Inc/Ametek | david.virissimo@ametek.com or 619-464-5430

Desert Canyon was named *2009 "Best Places to Play" by Golf Digest* and has been voted "*Best Public Golf Course" in Fountain Hills* for six consecutive years. A shuttle will pick up golfers at the Radisson Fort McDowell at 12:00 pm. Golfers will tee off shortly after arriving at the course. Golfers are welcome to drive themselves to arrive earlier. An awards presentation and reception will be held immediately following golf. Special Awards and Activities tentatively planned: Closest to the Pin and Longest Drive

Sponsorship Opportunities Available, details online at www.imaps.org/DevicePackaging/golf2013.htm.

Premier Golf Sponsors:

Premier - "Eagle" Sponsor:	Premier - "Eagle" Sponsor:	Premier - "Birdie" Sponsor:
SSEC	ASE GROUP	Amkor Technology

Golf Hole Sponsors:

SSEC | ASE GROUP | Amkor Technology | NAMICS | Infinite Graphics | SETNA | invensas | COINING. | AGC

WEDNESDAY, MARCH 13, 2013 — Afternoon Technical Sessions

	Advanced 3D Packaging	Flip Chip & Wafer Level Packaging	Advanced 3D Packaging 2
	WP1: **Processing Challenges & Solutions for 3D Packages** Chairs: Laura Mauer, Solid State Equipment Corp.; Rozalia Beica, Lam Research	WP2: **Wafer Level Fan-Out Packages & Materials** Chairs: Eric Huenger, Dow Chemical; Curtis Zwenger, Amkor	WP3: **Stress & Thermal Management in 3D IC Processing** Chairs: Gilles Poupon, CEA Leti; Keith Cooper, SETNA
2:30 pm - 3:00 pm	Fabrication of 3D-IC Interposers John Keech, Corning Inc. (Garret Piech, Scott Pollard)	Robust Reliability Performance of Large Size eWLB (Fan-out WLP) Seung Wook Yoon, STATSChipPAC, Ltd.	A Process Dependent Warpage and Stress Model for 3D Packages Considering Incoming Die/Substrate Warpage and Assembly Process Impacts Wei Lin, Amkor Technology (Ahmer Syed, KiWook Lee, Karthikeyan Dhandapani)
3:00 pm - 3:30 pm	Low Temperature MOCVD TiN Barrier Deposition for High Aspect Ratio TSVs : A Solution for 3D Integration Thierry Mourier, CEA-LETI Minatec (Stephane Minoret, Larissa Djomeni , Sylvain Maitrejean, Anne Roule, Laurent Vandroux; Sabrina Fadloun, Steve Burgess, Andy Price, Chris Jones, SPTS Technologies SAS)	Reliability and Performance Improvements of 3D System-in-Packages in Fan-Out Wafer Level Packaging Scott Hayes, Freescale (Tony Gong, Doug Mitchell, Michael Vincent, Jason Wright, Yap Weng Foong)	The Underfill-Microbump Interaction Mechanism in 3D ICs: Impact and Mitigation of Induced Stresses Andrej Ivankovic, IMEC (V. Cherman, M. Gonzalez, K.J. Rebibis, A. La Manna, G. Van der Plas, G. Wei, B. Vandevelde, I. De Wolf, G. Beyer , E. Beyne, D. Vandepitte)
3:30 pm - 4:00 pm	Through Si Vias Using Liquid Metal Conductors for Re-workable 3D Electronics George Hernandez, Auburn University (Daniel Martinez, Stephen Patenaude, Charles Ellis, Michael Palmer, Michael Hamilton)	Innovative 3D Structures Utilizing Wafer Level Fan-Out (WLFO) Technology Curtis Zwenger, Amkor Technology (JinYoung Khim, YoonJoo Khim, SeWoong Cha, SeungJae Lee, JinHan Kim, Amkor Technology, Korea)	TSV Delamination Risk Reduction and Stress Optimization through Improved Low-Temperature Cu Anneal Process Fengda Sun, Semiconductor Manufacturing International (Guangyu Sun, Hongbo Zhao, Xiaojun Chen, Xuanjie Liu, Xuejie Shi, He Huang)
4:00 pm – 4:30 pm	**Break in Exhibit Hall**		
4:30 pm - 5:00 pm	Strain in Electroless Copper Films: Analysis by In Situ X-Ray Diffraction and Curvature Methods Simon Bamberg, Atotech Deutschland GmbH (Tobias Bernhard (Laurence Gregoriades, Frank Bruning, Ralf Broening, Johannes Etzkorn, Wolfgang Friz, Michael Merschky, Bruce Muir, Laura Perry, Tanu Sharma)	A New Embedded Package Structure and Technology for the Next Generation of WLP, the Wafer level Fun-Out Package - WFOP (TM) Akio Katsumata, J-Devices Corporation	Thermal & Mechanical Challenges for 3DIC Integration Séverine Chéramy, CEA-LETI
5:00 pm - 5:30 pm	Extending the Strip Window for Advanced Packaging Photoresists Mani Sobhian, TEL NEXX	Development of a Low Residual Stress and High Performance Dielectric for WLP (Wafer Level Packaging) Applications Raymond Thibault, Dow Electronic Materials (Michael Gallagher, Kevin Wang, Matthew Yonkey, Duane Romer, Xiang Qian Liu, Kim Ho, Greg Prokopowicz, Joe Lachowski, Mark Oliver, Eric Huenger, Seiji Inaoka, Scott Kisting, Lynne Mills, Sue McNamara, Rosemary Bell)	Thermal Performance Evaluation of xFD Packages Ron Zhang, Invensas Corporation (H. Shaba, J. Tseng, E. Chau, W. Zohni, L. Mirkarimi)
5:30 pm - 6:00 pm	Copper, Nickel, and Lead-Free Solder Electroplating Solutions for Pillar and Micro-Pillar Capping Applications Julia Woertink, Dow Electronic Materials (Erik Reddington, Inho Lee, Yi Qin, Jonathan Prange, Pedro Lopez Montesinos, Jui-Ching Lin, Masaaki Imanari, Jianwei Dong, Wataru Tachikawa, Jeff Calvert)	Lead Free Paste with Under 3um Solder Particles for Fine Pitch C4 Bumping and Pre-Coating Solder Applications Hironori Uno, Mitsubishi Materials Corporation (Masayuki Ishikawa, Akihiro Masuda, Hiroki Muraoka, Kanji Kuba)	Techniques and Tools for Collaborative Thermal and Mechanical Modeling of 3D ICs Kamal Karimanal, Cielution LLC
6:00 pm – 7:30 pm	**Panel Discussion: 3D Integration - Applications and Production Challenges** Please join us for an interactive panel discussion on 3D Integration - Applications and Production Challenges. An executive panel has been assembled from several of the leading microelectronics organizations from around the world to discuss the latest **applications, trends in the industry, challenges, reliability, and production readiness.** The panel will be soliciting questions from the audience. **Moderators: Rozalia Beica, Lam Research AG; Peter Ramm, Fraunhofer EMFT** **Panelists:** Sitaram Arkalgud, Invensas; Rich Rise, ASE US; Arif Rahman, Altera *Additional panelists to be announced soon*		

Hotel Deadline: February 8, 2013

Rates and availability will not be guaranteed after the deadline – www.imaps.org/devicepackaging

Early Registration Deadline: February 8, 2013

All registration fees increase after the deadline.

$100 "Combo" Discount:

When you register for the "***Combo Registration***" for Device Packaging & the Global Business Council Conference (GBC).

THURSDAY, MARCH 14, 2013 — Technical Sessions

7:00 am – 11:30 am	**Registration**		
7:00 am – 8:00 am	**Continental Breakfast**		
8:00 am – 8:45 am	**KEYNOTE – 3D** ***2.5 D Options: Organic Vs. Silicon.Vs Glass; Technologies, Costs and Applications*** *Dr. Rao R .Tummala, Director PRC* GEORGIA INSTITUTE OF TECHNOLOGY **Abstract**: Transistor scaling, starting with the invention of transistor in 1940s, made electronics the largest global industry, serving a variety of individual industries that span computing, communications, consumer, automotive and others . A new industry that integrates all these into so-called Smart Mobile Systems promises to be the next frontier in electronics hardware, performing every imaginable function in smallest size and lowest cost that every global person could afford. Such revolutionary systems, however, require revolutionary technologies referred to as system scaling, in contrast to transistor scaling during the last 60 years. Current hardware approaches based on organic laminates has four main limitations: 1) lithographic ground rules, 2) thermal performance, 3) mismatch in TCE-driven, and moisture-driven reliabilities, and 4) warpage, as these are processed as ultra-thin packages. Inorganic packages such as Glass or Silicon address these fundamental problems. These can be combined appropriately and selectively with ultra-thin and special polymers as dielectrics, liners and stress-relief members. This presentation will try to clarify the role and regimes of each of these organic, silicon and glass interposers for 2.5 and 3D applications. ***Professor Rao Tummala*** *is a Distinguished and Endowed Chair Professor, and Founding Director of NSF ERC, called PRC at Georgia Tech, known as the world's premier systems packaging Center pioneering System Scaling technologies, producing the most cross-disciplinary engineers and transferring both to global industry. Prior to joining Georgia Tech, he was an IBM Fellow, pioneering the first plasma display and low temperature co-fired(LTCC) multichip electronics for mainframes and servers. Prof. Tummala published about 500 technical papers, holds 90 patents and inventions; authored the first modern Microelectronics Packaging Handbook, the first undergrad textbook, "Fundamentals of Microsystems Packaging", and first book introducing the System-On-Package technology. His Georgia Tech PRC Center is considered the number 1 Academic Center having produced more than 1000 Ph.D, MS and BS students, 2000 publications and collaborating with more than 100 companies in US, Europe, Japan and Korea. He is a Fellow of IEEE, and a member of National Academy of Engineering in US and India . He was a past President of IEEE-CPMT and the IMAPS Societies.*		
8:45 am – 9:30 am	**KEYNOTE – 3D** ***Future of Package for Computing Electronics*** *Ram S. Viswanath, Assembly Technology Planning and Pathfinding* INTEL CORPORATION **Abstract**: Computing, communication and entertainment media have rapidly converged creating a wide range of "smart" devices, driven by the Internet and the need and desire to be "always connected." New device categories are emerging at a rapid pace to bring computing experiences into every aspect of our lives. Consumers are demanding consistency and interoperability across all of their devices, from phone to PC to tablet to TV to gadget, making computing a seamless experience regardless of where you are, what you are doing or what your needs at the time may be. This computing continuum or convergence is predicted to result in more than 10B connected devices by 2015 with significant challenges and opportunities for microelectronic packaging. This presentation will focus on explaining these challenges and potential future solutions with regard to increased demand for memory bandwidth, multi functionality, and higher wiring density to meet the Si scaling requirements, thinner and smaller form factors, multi-chip and embedded packaging while also addressing the challenges associated with demand for lower cost and environmental sustainability. ***Ram Viswanath*** *leads the Package Architecture and Technology Definition for all Intel products. He has been with the Assembly and Test Technology organization for the past twenty years. His recent focus is in developing ultra thin small form factor packaging for mobile computing and high performance interconnects for server CPU's. He has numerous patents in the areas of thermal sciences, sockets, high speed interconnects and 3D packaging. Ram received his doctorate from Rutgers University in Mechanical and Aerospace Engineering.*		
9:30 am – 9:45 am	**Break in Foyer**		
	Advanced 3D Packaging	**Flip Chip & Wafer Level Packaging**	**Advanced 3D Packaging 2**
	THA1: **Reliability Considerations in 3D Packaging** Chairs: Severine Cheramy, CEA Leti; James Lu, Rensselaer Polytechnic Institute	THA2: **Applications of FC & WLP Packages** Chairs: Scott Hayes, Freescale; Jon Aday, FlipChip International	THA3: **3D and WLP Metrology & Inspection** Chairs: Jianwei Dong, Dow Chemicals; Rozalia Beica, Lam Research
9:45 am – 10:15 am	Integration, Electrical Performance and Reliability Investigation of TSV Shih-Wei Lee, National Chiao Tung University (Yu-Chen Hu, Cheng-Hao Chiang, Kuo-Hua Chen, Chi-Tsung Chiu, Ching-Te Chuang, Wei Hwang, Jin-Chern Chiou, Ho-Ming Tong, Kuan-Neng Chen)	High Reliability Fine Pitch WLCSP David Lawhead, FlipChip International (Ronnie Yazzie, Tony Curtis, Guy Burgess, Ted Tessier)	Multi-Scale Materials Data for 3D TSV Stack Performance Simulation and Model Validation Ehrenfried Zschech, Fraunhofer IZFP (Kong Boon Yeap, Christoph Sander, Uwe Mohle, Fraunhofer IZFP-D; Valeriy Sukharev, Mentor Graphics)
10:15 am – 10:45 am	The Reliability Study of a High Density Multi Chip Packaging with Folding Flexible Substrate Yin Wen, Inst. of Micro., Chinese Academy of Sciences (Bo Zhang, Yuan Lu, Liao Anmou, Du Tianmin, Lixi Wan)	RF Devices: from WLSCP to Smart Interposers Yann Lamy, CEA-LETI (O. El Bouayadi, C. Ferrandon, S. Joblot, A. Jouve, L. Dussopt, T. Lacrevaz, C. Bermond, B. Flachet, G. Simon)	Metrology and Inspection of 3D IC TSV Integration Processes G. Fresquet , Fogale NANOTECH
10:45 am – 11:15 pm	Ultra-Fine Pitch Package on Package Solution for High Bandwidth Mobile Applications Rajesh Katkar, Invensas Corp. (Zhijun Zhao, Ron Zhang, Rey Co, Laura Mirkarimi)	Electrical Characterization on a High-Speed Wafer-Level Package Kai Liu, STATSChipPAC (YongTaek Lee, HyunTai Kim, MaPhooPwint Hlaing, Susan Park, Billy Ahn)	Discover, Analyze and Monitor Yield-limiting Events in a WLP process Reza Asgari, Rudolph Technologies
11:15 am – 11:45 am	Overview of Critical 3D Integration Challenges to Bring Products to Market Douglas Coolbaugh, University of Albany, College Of Nanoscale Science and Engineering (Daniel Pascual, Colin McDonough, Joseph Piccirillo Jr., Michael Liehr)	Advanced Microelectronics Packaging Solutions for Miniaturized Medical Devices Rabindra Das, Endicott Interconnect Technologies (Steven Rosser, Frank Egitto)	An Innovative 2.5D IC Interconnection Reliability System Doug Goodman, Ridgetop Group (Andrew Levy , Hans Manhaeve, Ridgetop; Ed McBain, ALLVIA)
11:45 am – 12:00 pm	**Closing Remarks** (In Main 3D Session Room)		
1:15 pm – 7:00 pm	**IMAPS Microelectronics Foundation Spring Golf Invitational** **Desert Canyon Golf Club - 1:15 pm Shotgun Start - *"Best Ball" Scramble*** **(Separate Registration - www.imaps.org/DevicePackaging/golf2013.htm)**		

Device Packaging Exhibition and Technology Showcase

"An opportunity to talk to industry leaders"

Device Packaging 2013 will feature one collective Exhibition and Technology Showcase for vendors and suppliers who support the many aspects of Device Packaging and each of the topical areas addressed during this Conference. This venue features an ideal atmosphere for exhibiting companies to showcase their products and services to key decision making professionals in the industry and for a large focused audience of attendees to engage these companies about the solutions they need. ***Full 8' by 10' exhibit booths will be on display.***

There is only one exhibit booth still available in the hall – ***1 BOOTH REMAINS!*** The exhibits have sold out each of the past seven years, and will sell out again this year. If you have questions about exhibiting with IMAPS, or about getting signed up for the 2013 Device Packaging Conference, contact Brian Schieman at bschieman@imaps.org (202-548-8715). Online at http://www.imaps.org/DevicePackaging/exhibits13.htm.

Exhibit Hours:

Tuesday - March 12 **10:00 am - 7:00 pm**
Refreshment Breaks, Lunch, and a Reception will be held in the Exhibit Hall.

Wednesday - March 13 **12:00 pm - 4:30 pm**
Refreshment Breaks, Lunch and a Poster Session will be held in the Exhibit Hall.

For more information, visit:
www.imaps.org/devicepackaging or contact IMAPS at *202-548-8715*

Exhibitors on the Device Packaging 2013 USB

IMAPS is offering Exhibiting Companies the opportunity to have an unlimited amount of product promotion information on the Conference USB. **You must submit ONE PDF, Word or Powerpoint file, via e-mail, containing the information you want to appear to bschieman@imaps.org on or before March 14, 2013.** Files must be sent to Brian Schieman (bschieman@imaps.org). Submissions must be as stated and arrive by the deadline. There is no charge for participation.

Conference USB

If you are unable to attend the Conference and would like a copy of the USB of Presentations, you may purchase a copy by using the registration form. Your copy will be mailed to you after the event.

The cost is $200 for members; $300 for nonmembers,* plus shipping and handling.

Reserve your copy on-line at
www.imaps.org/devicepackaging or call 202-548-4001.

Conference Hotel

RADISSON FORT MCDOWELL RESORT & CASINO
10438 NORTH FORT MCDOWELL ROAD
SCOTTSDALE/FOUNTAIN HILLS, AZ 85264
PHONE: 480-789-5300 OR 800-333-3333
By Phone: please reference *IMAPS* or *IMAPS Device Packaging*

$155/night single/double
Register On-line at:
http://www.radisson.com/reservation/resEntrance.do?pacLink=Y&promoCode=IMAP13&hotelCode=AZMCDOWE

Hotel Deadline: February 8, 2013
Rates and availability will not be guaranteed after the deadline.

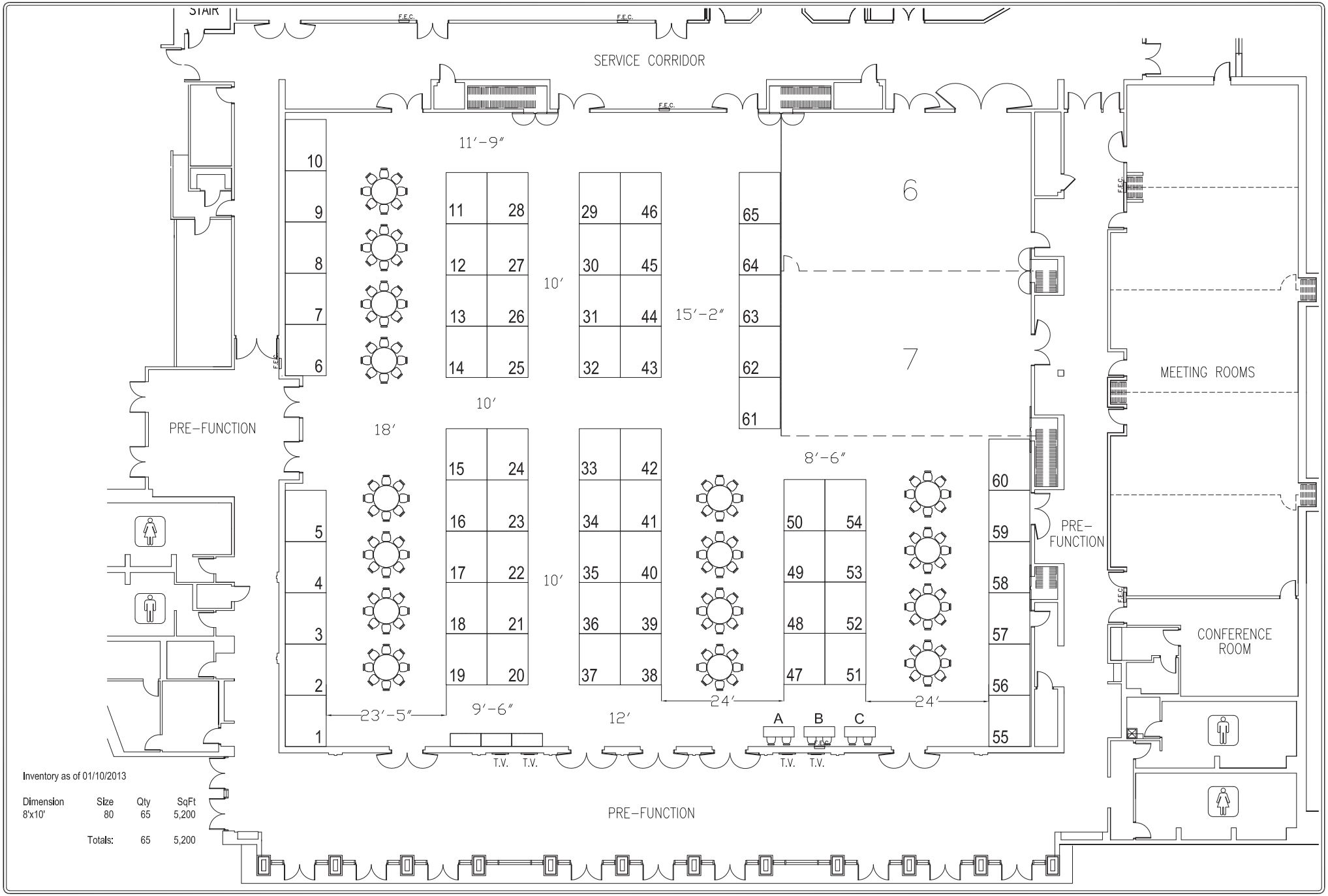
Device Packaging Exhibition and Technology Showcase

Exhibiting Companies *(as of January 24, 2013)*

The exhibit hall is nearly sold out, with only ***ONE BOOTH*** still available. The following booths will be on display during Device Packaging 2013. Please visit the companies' websites listed below for more information. A floor plan of the exhibit hall can be found on page 19. If you have questions about exhibiting with IMAPS, or about getting signed up for the 2013 Device Packaging Conference, contact Brian Schieman at bschieman@imaps.org or 202-548-8715.

Company	Booth(s)	Company	Booth(s)	Company	Booth(s)
3D Plus USA www.3D-plus.com	51	Endicott Interconnect Technologies www.endicottinterconnect.com	06	PVA TePla America, Inc. www.pvateplaamerica.com	59
ACM Research, Inc. www.acmrcsh.com	29	F&K Delvotec, Inc. www.fkdelvotecusa.com	58	Riv, Inc. www.rivinc.com	30
AdTech Ceramics www.adtechceramics.com	26	Finetech, Inc. www.finetechusa.com	25	Rudolph Technologies, Inc. www.rudolphtech.com	55
AGC Electronics America www.agcem.com	13	FRT of America, LLC www.frtofamerica.com	07	SANTIER www.santier.com	34
AI Technology, Inc. www.aitechnology.com	35	Hesse Mechatronics www.hesse-mechatronics.us	01-02	Sentec Electro Ceramic & Device Group www.sentecee.com	40
ALLVIA, Inc. www.allvia.com	39	IMAT, Inc. www.imatinc.com	05	SETNA www.set-na.com	45
Amicra Microtechnologies GmbH www.amicra.com	63	Infinite Graphics www.igi.com	19	Sikama International, Inc. www.sikama.com	21
Amkor Technology **www.amkor.com**	**47**	Interconnect Systems, Inc. www.isipkg.com	48	**Solid State Equipment Corporation** **www.ssecusa.com**	**38**
ASE Group **www.aseglobal.com**	**50**	Kyocera America, Inc. www.kyocera.com/kai/semiparts	22	Sonoscan, Inc. www.sonoscan.com	61
ASM Pacific Technology, Ltd. www.asmpacific.com	62	LINTEC OF AMERICA, INC. www.lintec-usa.com	27	STATS ChipPAC, Inc. www.statschippac.com	52
Atotech USA, Inc. www.atotech.com/en/region/americas/usa.html	33	Micro Hybrid Dimensions, Inc. www.micro-hybrid.com	23	Surfx Technologies www.surfxtechnologies.com	08
Axus Technology www.axustech.com	16	Micross Components www.micross.com	64	TDI International www.tdiinternational.com	11
Azimuth Electronics, Inc. www.azimuth-electronics.com	41	Mini-Systems, Inc. www.mini-systemsinc.com	31	TechSearch International, Inc. www.techsearchinc.com	37
Boschman Technologies / Advanced Packaging Center www.boschman.com	49	Mitsubishi Materials Corporation www.mmus.com	24	Teledyne Microelectronic Technologies www.teledynemicro.com	46
Chalman Technologies, Inc. www.cti-rep.com	03-04	NAMICS Corporation www.namics.co.jp	42	Trace Laboratories, Inc. www.tracelabs.com	09
Cleanlogix LLC www.cleanlogix.com	57	nMode Solutions, Inc. www.nmodesolutions.com	12	Unisem Group www.unisemgroup.com	18
CMS Circuit Solutions, Inc. www.cmscircuitsolutions.com	65	Oneida Research Services, Inc. www.ors-labs.com	28	West Bond, Inc. www.westbond.com	43
CPS Technologies Corporation www.alsic.com	53	Pac Tech Packaging Technologies USA www.pactech-usa.com	54	XIA, LLC www.xia.com	17
Dow Electronic Materials www.rohmhaas.com/electronicmaterials	36	Palomar Technologies, Inc. www.palomartechnologies.com	32	XYZTEC www.xyztec.com	44
DYCONEX AG www.mst.com/dyconex Micro Systems Engineering GmbH www.mst.com/msegmbh	15 *(shared)*	Polysciences, Inc. www.polysciences.com	56	Yolé Developpement www.yole.fr	14
Dynaloy www.eastman.com	60	Pure Technologies, LLC www.puretechnologies.com	20	***Thank You to the 2013 Exhibitors!*** **The Exhibit Hall has SOLD OUT for the past 7 years and is expected to sell out again!** **Reserve your space today:** **bschieman@imaps.org**	

Thank you to the Device Packaging Premier Sponsors:



Inventory as of 01/10/2013

Dimension	Size	Qty	SqFt
8'x10'	80	65	5,200
Totals:		65	5,200

GES Global Experience Specialists

9th International Conference and Exhibition on Device Packaging

March 12-13, 2013

Radisson Fort McDowell Resort & Casino

Ballrooms 1-5, 8-9

File: IDPC 1303 RADFTM.dwg
Plotted: Jan 10, 2013
By: BURTOC

EVERY EFFORT HAS BEEN MADE TO INSURE THE ACCURACY OF ALL INFORMATION CONTAINED ON THIS FLOOR PLAN. HOWEVER, NO WARRANTIES, EITHER EXPRESSED OR IMPLIED, ARE MADE WITH RESPECT TO THIS FLOOR PLAN. IF THE LOCATION OF BUILDING COLUMNS, UTILITIES, OR OTHER ARCHITECTURAL COMPONENTS OF THE FACILITY IS A CONSIDERATION IN THE CONSTRUCTION OR USAGE OF AN EXHIBIT, IT IS THE SOLE RESPONSIBILITY OF THE EXHIBITOR TO PHYSICALLY INSPECT THE FACILITY TO VERIFY ALL DIMENSIONS AND LOCATIONS.

A Decade of TSV Development*

* January 2000, Solid State Technology Magazine

MOORE'S LAW – THE Z DIMENSION

"Investment in technologies that provide both wafer-level vertical miniaturization (wafer thinning) and preparation for vertical integration (through-silicon vias) makes good sense." Sergey Savastiouk, Allvia CEO

December 2008, Solid State Technology Magazine

MOORE'S LAW – THE Z DIMENSION: A DECADE LATER

"There are five steps to be analyzed: feasibility, niche applications, reliability, cost reduction, and high-volume production." Savastiouk

ALLVIA

Through-Silicon Via Foundry

www.allvia.com

Introducing...

SANTIER®

Engineered Microelectronic Housings & Assemblies

We Don't Just Manufacture Microelectronic Housings & Assemblies... We Expand Your Expectations.

***SANTIER**, formerly PlanseeTMS (PTMS), plans expansion of services and capacity for its build-to-spec electronic device packages.*

If you are a design engineer looking for precise solutions from a trustworthy partner, Santier is the world-class designer and manufacturer of micro-electronic housings and assemblies from custom engineered materials.

We Solve Your Problems.

Santier has the technical expertise to entrust your mission critical projects—when you need it—on budget and at the highest quality, so you are confident your product will work the first time, every time.

Connect With Us At The IMAPS Show.

Critical projects require exceptional thinking—see for yourself why we're the most trusted leader in microelectronic packaging.

Call us for a plant tour or visit Booth # 34 at IMAPS 2013

Commitment Beyond Our Part

www.Santier.com

858-271-1993 • 10113 Carroll Canyon Road • San Diego, CA 92131, USA

IMAPS 2013

46th International Symposium on Microelectronics

Bringing Together the Entire Microelectronics Supply Chain!™

Rosen Centre Hotel, Orlando, Florida - USA

September 29 - October 3, 2013

The 46th International Symposium on Microelectronics will be held at the Rosen Centre Hotel in Orlando, Florida, USA, and is being organized by the International Microelectronics And Packaging Society (IMAPS). The IMAPS Technical Committee seeks original papers that present progress on technologies throughout the entire microelectronics/packaging supply chain. The 46th Symposium on Microelectronics will cover three tiers of electronics: Systems and Applications; Design and Related Measurements; and Materials, Process and Reliability. IMAPS 2013 will feature 5-6 technical tracks that span the three days of sessions on: **3D IC/Packaging; Modeling, Design & Reliability; Next Generation Materials; Advanced Technologies; Advanced Packaging; Assembly and Packaging**; as well as Invited/Translated Sessions and an Interactive/Academic Poster Session and more.

Sessions are being planned and abstracts will be considered on the topics listed below. Abstracts are rated by the technical committee members and are selected into the sessions by the session chairs appointed by the technical committee. Authors should identify their preferred session (topical area) when submitting their abstracts. Abstracts should highlight the major contributions of the work in one or more of these areas. **All abstracts submitted must represent original, previously unpublished work.**

General Chair:
Matt Nowak
Qualcomm, Inc.
mnowak@qualcomm.com

Technical Chair:
Ivan Ndip
Fraunhofer IZM
Ivan.Ndip@izm.fraunhofer.de

Industries Represented

- Consumer, Portable, and Wireless
- Biomedical
- Telecom
- Defense and Security
- Computing and Gaming
- Automotive, Industrial, Harsh Environment Electronics Applications

Systems & Applications

- Low Cost Electronics
- Outsourcing and Supply Chain Management
- Thermal Management
- System Packaging
- Power Management
- Electromagnetic Interference (EMI)
- Electrostatic Discharge (ESD) Protection
- Wireless Sensors and Energy Harvesters
- Nano-Integrated Packaging
- Microwave & RF Applications
- Photonic Packaging
- Packaging for Harsh Environments
- MEMS Packaging
- Biological and Microfluidic Packaging

Interactive Student Poster Session

Student papers will be considered for the interactive session.

Design and Related Measurements

- 2.5 & 3D Packaging Approaches
- 3D Simulation and Modeling
- Electrical Modeling, Signal & Power Integrity
- Mechanical Modeling and Related Metrology
- High Performance Interconnects and Boards
- Embedded and Integrated Passives
- Wafer Level Packaging / CSP

Materials, Process, and Reliability

- Flip-Chip, Copper Pillar, TSV, Wafer Thinning, Wafer Bumping
- 2.5D Silicon/Glass Interposers and 3D Direct Chip Stacking
- Polymers, Underfill/Encapsulants and Adhesives
- Advanced Materials and Novel Assembly Processes
- Thick / Thin Films
- Warpage Characterization and Mitigation
- Pb-Free Solder Materials, RoHS
- Packaging Reliability Testing
- Wirebonding and Stud Bumping

"Invited" Sessions

The following special sessions are being considered for IMAPS 2013 and speakers will be invited along these areas:

- European and Asian Perspectives on Packaging and System-Integration
- Microelectronics Activity in the South-East US (Military, Bio-Medical, Wireless, and other topics)

Please send your 500 word abstract **electronically only** using the on-line submittal form at: www.imaps.org/abstracts.htm. **All Speakers are required to pay a reduced registration fee.** If you need assistance with the on-line submission form, please email Brian Schieman (bschieman@imaps.org) or call 202-548-8715.

Abstract Cut-off Date: March 15, 2013 | **Notice of Acceptance: April 30, 2013** | **Final Manuscript Due: July 15, 2013**

Special Paper Recognition - Cash Awards Offered!

6 "Best of Track" Outstanding Papers - Six $500 Cash Awards

1 "Best Paper of Symposium" - One "best of track" winner receives additional $500 award

Best Paper of Sessions are considered for Best of Symposium and Outstanding Papers

IMAPS Microelectronics Foundation Student Paper Awards

The Foundation is offering cash awards to the best papers submitted and presented by students at IMAPS 2013.

IMAPS Calendar of Events *(as of January 23, 2013)*

Event	Start Date	End Date	Event Description
2013 Conference and Exhibition on Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT)	4/23/2013	4/25/2013	IMAPS/ACerS 2013 Conference and Exhibition on Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT) www.cicmt.org **Early Registration/Hotel Deadline: March 22, 2013**
2nd Advanced Technology Workshop and Tabletop Exhibits on Packaging the Next Generation of Nano Devices	4/30/2013	5/1/2013	With each new generation of high density devices, the packaging community faces ever more difficult challenges. These "nano" topics will be addressed at this workshop to be held at the College of Nanoscale Science and Engineering (CNSE) in Albany, New York. www.imaps.org/nano **Abstract Deadline: March 8, 2013**
New England Chapter's 40th Annual Symposium and Exposition	5/7/2013	5/7/2013	New England Chapter's 40th Annual Symposium and Exposition. Tuesday, May 7, 2013 in Boxborough, MA www.imapsne.org
Advanced Technology Workshop and Tabletop Exhibition on Microelectronic Packaging for Medical and Hi-Rel Devices	5/13/2013	5/14/2013	This ATW will be held in Downtown Minneapolis. The combination of advancing demographics (an aging world population) and an explosion of new micro-electronics technology set the stage for significant improvement and miniaturization in the area of medical electronics. www.imaps.org/medical **Abstract Deadline: March 22, 2013**
Advanced Technology Workshop and Tabletop Exhibition on Advanced Electronics for Mobile Energy Systems (AEMES)	6/6/2013	6/7/2013	IMAPS and the Space Coast Energy Consortium present the first annual AEMES Workshop to be held at the FL Solar Energy Center in Cocoa, Florida. www.imaps.org/energy **Abstract Deadline: March 29, 2013**
HiTEN 2013 - High Temperature Electronics Network	7/8/2013	7/10/2013	HiTEN 2013 International Conference and Exhibition on High Temperature Electronics Network www.imaps.org/hiten **Early Registration/Room Deadline: June 14, 2013**
IMAPS 2013 - 46th International Symposium on Microelectronics	9/29/2013	10/3/2013	IMAPS 2013 will be held at the Rosen Centre, Orlando, Florida, USA, and is being organized by the International Microelectronics Assembly and Packaging Society. www.imaps2013.org **Abstract Deadline: March 15, 2013**

Get Published With IMAPS!

We invite you to submit your technical manuscript(s) for peer review for an upcoming issue of the ***Journal of Microelectronics and Electronic Packaging (JMEP)***.

The IMAPS Journal is a prestigious, refereed, and archival publication distributed to a qualified audience worldwide comprised of IMAPS members, educational institutions, and corporate libraries. Focused solely on microelectronics topics and the electronic packaging of these technologies, JMEP contains only papers relevant to your business and industry.

Complete information regarding this publication may be found on the IMAPS website at www.imaps.org/jmep; however, the key points are:

- With such a technically focused publication, you can get to print much faster with JMEP – 3-4 months on average from submission to publication.
- All submissions must be in electronic format, and should be submitted via E-Mail to jmep@imaps.org.
- Papers should preferably be formatted and submitted in Microsoft Word.
- Tables, graphs, and photographs should be submitted at the end of the file and need not be embedded in the text.
- Photographs and other illustrations should preferably be submitted as high resolution files - JPEG, GIF or WMF format preferred.
- The Transfer of Copyright form must be filled out on the IMAPS website. http://www.imaps.org/jmep/copyright.pdf.

Authors of *non-published papers* that have been printed in other IMAPS publications or presented at IMAPS workshops are invited to submit updated and/or expanded versions of their papers for possible publication in the Journal.

Please send all submissions, comments, or questions to jmep@imaps.org or feel free to contact the phone/e-mail below.

IMAPS
611 2nd Street, NE
Washington, DC 20002
Phone: 202-548-8715
E-mail: bschieman@imaps.org
Website: www.imaps.org/jmep

Everything in electronics between the chip and the system!

Program at a Glance

Sunday, March 10

Registration and GBC Welcome Reception: 5:30 pm - 7:00 pm
Speaker Dinner *(by Invitation)*: 7:00 pm - 9:00 pm

Monday, March 11

Registration and Continental Breakfast: 7:00 am - 8:00 am
GBC Conference & PDCs: 8:00 am - 5:00 pm

Device Packaging Conference Professional Development Courses (PDC) - (1/2 Day)
8:00 am - Noon

PDC1
2.5D/3D, Flip Chip WLP, MEMS & LED Packaging Trends, Updates & Advances
Course Leader: Phillip G. Creter, Creter & Associates

PDC2
Recent Advances in Glass & Silicon Interposers for 2.5D and 3D Integration
Course Leader: Venky Sundaram, Georgia Institute of Technology (PRC)

PDC3
High-Temperature Electronics - with an Emphasis on Assembly & Packaging
Course Leader: Randall Kirschman, Consultant

PDC4
Hermetic Sealing and Testing of Small Volume MEMS Packages
Course Leader: Thomas J. Green, TJ Green Associates LLC

PDC5
Failure Mode Analysis of Flip Chip and Advanced Package and Board Assemblies
Course Leader: Daniel Baldwin, Engent, Inc.

Device Packaging Conference Professional Development Courses (PDC) - (1/2 Day)
1:00 pm - 5:00 pm

PDC6
Fundamentals of Glass Technology and Applications for Advanced Semiconductor Packaging
Course Leader: TJ Kiczenski, Corning, Inc.

PDC7
Polymers for Electronic Packaging
Course Leader: Jeffrey Gotro, InnoCentrix, LLC

PDC8
Thermal & Mechanical Simulation Techniques - An Introductory Course for 3D Enablement Professionals
Course Leader: Kamal Karimanal, Cielution LLC

PDC9
MEMS Reliability and Packaging
Course Leader: Slobodan Petrovic, Oregon Institute of Technology

PDC10
Basics of Conventional and Advanced Packaging
Course Leader: Syed Sajid Ahmad, Center for Nanoscale Science and Engineering, NDSU

Welcome Reception: 5:15 pm - 6:45 pm

2013 Texas Hold'em Tournament: 7:00 pm - 10:00 pm

Visit http://www.imaps.org/DevicePackaging/holdem2013.htm for more information. (Limited Seating)
To Benefit the IMAPS Microelectronics Foundation

Tuesday, March 12

7:00 am - 7:00 pm
Registration

8:20 am - 9:55 am
Keynote Presentations

10:00 am - 7:00 pm
Exhibits Open

10:30 am - 12:30 pm
Technical Session
TA1-TA3

12:30 pm - 2:00 pm
Lunch Break In Exhibit Hall
(Food served from 12:30 pm - 1:30 pm)

2:00 pm - 5:45 pm
Technical Sessions
TP1-TP3

5:45 pm - 7:00 pm
Reception In Exhibit Hall

7:00 pm - 8:30 pm
Panel Discussion: Flip Chip & Wafer Level Packaging

Wednesday, March 13

7:00 am - 6:00 pm
Registration

8:00 am - 9:30 am
Keynote Presentations

10:00 am - 12:30 pm
Technical Sessions
WA1-WA3

12:30 pm - 2:30 pm
Lunch Break In Exhibit Hall
(Food served from 12:30 pm - 1:30 pm)

12:00 pm - 4:30 pm
Exhibits Open

2:00 pm - 4:30 pm
Poster Session in Exhibit Hall
(Poster setup: 1:30 pm - 2:00 pm)

2:30 pm - 6:00 pm
Technical Sessions
WP1-WP3

6:00 pm - 7:30 pm
Panel Discussion:
3D Integration - Applications and Production Challenges

Thursday, March 14

7:00 am - 11:30 am
Registration

8:00 am - 9:30 am
Keynote Presentations

9:45 am - 11:45 am
Technical Sessions
THA1-THA3

11:45 am - 12:00 pm
Closing Remarks

1:15 pm - 7:00 pm
IMAPS Microelectronics Foundation Spring Golf Invitational
(Separate Registration)
Desert Canyon Golf Club (www.desertcanyongolf.com)
1:15 pm Shotgun Start
"Best Ball" Scramble
See page 14 for more information.

Registration Form

Register On-Line at www.imaps.org/devicepackaging

Device Packaging Conference - March 11 - 14, 2013

❑ Dr. ❑ Mr. ❑ Ms. Member ID# _____

First Name_____M.I._____Last Name_____

Company/Affiliation_____Job Position_____

Address_____

City_____ State_____ Zip_____ Country_____

Phone_____ Fax_____ Email_____

Payment DPC13

Device Conference Fee: $_____

GBC Only Fee: $_____

Combo Fee: $_____

Professional Development Course: $_____

Exhibit Booth Fee: $_____

Additional Purchases: $_____

Total Payment Due: $_____

❑ Enclosed is a check payable in US funds to IMAPS

Charge my fees to:

❑ AMEX ❑ VISA ❑ MC ❑ Discover

Card#_____ Exp._____

Signature _____

Card billing address, if different from above: (required)

_____

_____

Email address required to receive confirmation of registration.

For Wire Transfer information call 202-548-4001.

Mail this form with payment to: IMAPS * 611 2nd Street, NE * Washington, DC 20002-4909. For credit card transactions, register on-line: www.imaps.org; or register by phone with your credit card by calling 202-548-4001. Additional information? E-mail: bschieman@imaps.org, or visit our web site: http://www.imaps.org. Cancellations will be refunded (less a $50 processing fee) only if written notice is postmarked on or before **Friday, February 15, 2013**. No refunds will be issued after that date.

Presorted
First-Class Mail
U.S. Postage
PAID
Merrifield, VA
Permit No. 6418

IMAPS Registration
611 2nd Street, NE
Washington, DC 20002-4909

Registration Fees: Early Registration Ends 2/8/13

Device Conference Fees

	(On or before 2/8)	(After 2/8)
❑Member (IMAPS)*	$675	$775
❑Non-Member*	$775	$875
❑Speaker* ❑Chair* ❑Chapter Officer*	$425	$525
❑Student*	$275	$375
❑Exhibits Only (does not include lunch)	**FREE**	
Exhibit Lunch (per person/per day) ❑Tuesday ❑Wednesday	$30	

GBC Only:

❑Member (IMAPS)*	$550	$600
❑Non-Member*	$750	$800

Combo Fees (Register for both and save at least $100)

Device & GBC: **$100 savings already calculated in price below.**

❑Member (IMAPS)*	$1100	$1250
❑Non-Member*	$1400	$1550
❑Speaker* ❑Chair* ❑Chapter Officer*	$850	$1000
❑Student*	$450	$600

**Includes one-year IMAPS individual membership or membership renewal at no additional charge. Does not apply to corporate or affiliate memberships. Conference Fee includes access to all technical sessions, all meals listed, welcome reception, and one (1) USB of presentations; USB will contain the extended abstract and presentation as submitted by the presenter. USB will be mailed 15 business days after the event.*

Professional Development Courses - 1/2 Day

Monday, March 11: 8 am - Noon		
❑3D, FC/WLP, MEMS & LED Pckg Trends...PDC1	$400	$450
❑Glass & Silicon Interposers for 2.5/3D...PDC2	$400	$450
❑High Temperature Electronics...PDC3	$400	$450
❑Hermetic Sealing & Testing of MEMS Packages...PDC4	$400	$450
❑Failure Mode Analysis of Flip Chip & Adv Package...PDC5	$400	$450
Monday, March 11: 1 pm - 5 pm		
❑Fundamentals of Glass Tech & Apps for Semi Pkg...PDC6	$400	$450
❑Polymers in Semiconductor Packaging...PDC7	$400	$450
❑Thermal & Mechanical Simulation for 3D...PDC8	$400	$450
❑MEMS Reliability & Packaging...PDC9	$400	$450
❑Basics of Conventional & Adv Packaging...PDC10	$400	$450

Exhibit Booth (March 12 - 13)

❑IMAPS Corporate Member	$1300	$1500
❑Non-Corporate Member	$2000	$2200

Additional Purchases

❑Texas Hold'em Tournament *(Limited Seating)*	$50	$50
❑USB of Presentations *(Member Rate)*	$200	$200
❑USB of Presentations *(Non-Member Rate)*	$300	$300
❑Add to Ship	$7(US)	$25(Int.)

IMAPS Microelectronics Foundation Spring Golf Invitational
March 14 (*Separate Registration - See Page 14)*
Register On-Line at www.imaps.org/DevicePackaging/golf2013.htm

Housing *(Hotel Cut-off is February 8, 2013)*

Radisson Fort McDowell Resort and Casino
10438 North Fort McDowell Road
Scottsdale/Fountain Hills, AZ 85264
Phone: 480-789-5300

By Phone: please mention IMAPS or IMAPS Device Packaging

Online Reservations:

www.radisson.com/reservation/resEntrance.do?pacLink=Y&promoCode=IMAP13&hotelCode=AZMCDOWE

Single/Double: $155/night